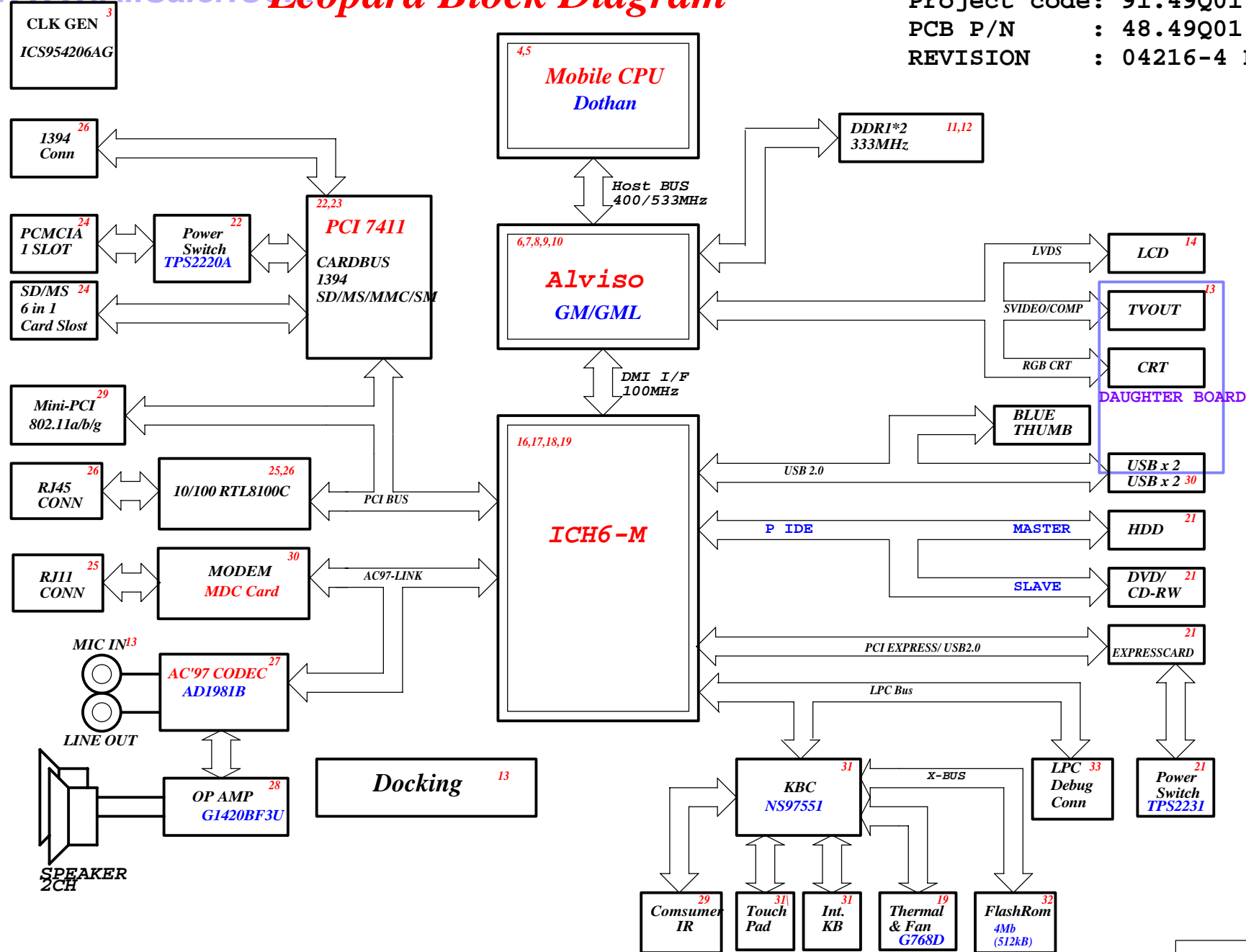


Project code: 91.49Q01.001
PCB P/N : 48.49Q01.021
REVISION : 04216-4 FF



SYSTEM DC/DC MAX1999	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5
SYSTEM DC/DC TPS5130	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D2V_S0 2D5V_S3

MAXIM CHARGER	
34	MAX1909
INPUTS	OUTPUTS
DCBATOUT	BT+
	18V 4.0A
	5V 100mA

CPU DC/DC	
35	MAX1907
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	VCC
L6:	Signal 4

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, EE_CS, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

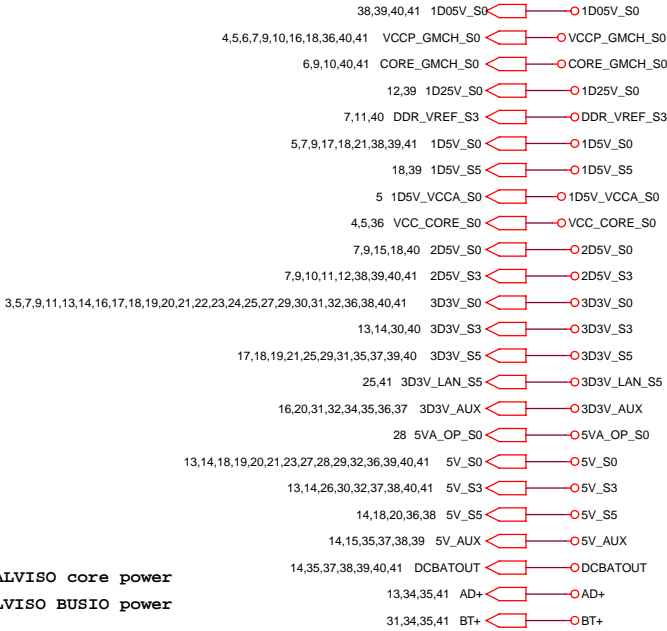
ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

Power name description

5V_S0= 5 Voltage power up on system work(S0 state)
5V_S3= 5 Voltage suspend to RAM(S3 state)
5V_S5= 5 Voltage soft off(S5 state)
3D3V_S0= 3.3 Voltage power up on system work(S0 state)
3D3V_S3= 3.3 Voltage suspend to RAM(S3 state)
3D3V_S5= 3.3 Voltage soft off(S5 state)
LVDDR_2D5V= 2.5 Voltage power up on system work(S0 state)
2D5V_S3= 2.5 Voltage suspend to RAM(S3 state)
2D5V_S0= 2.5 Voltage power up on system work(S0 state)

VCC_CORE_S0= CPU VID Voltage power up on system work(S0 state)
1D5V_VCCA_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S0= 1.5 Voltage power up on system work(S0 state)
1D5V_S5= 1.5 Voltage soft off(S5 state)
DDR_VREF_S3= 1.25 Voltage suspend to RAM(S3 state)
1D25V_S0= 1.25 Voltage power up on system work(S0 state)
1D2_VGA_S0= 1.2 Voltage power up on system work(S0 state) for VGA
1D05V_S0= 1.05 Voltage power up on system work(S0 state)
CORE_GMCH_S0= 1.05 Voltage power up on system work(S0 state) for ALVISO core power
VCCP_GMCH_S0= 1.05 Voltage power up on system work(S0 state)for ALVISO BUSIO power



PCI RESOURCE TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#
Mini-PCI	AD21	P_INTE#	REQ0# / GNT0#
Cardbus Controller TI7411	AD22	(CARBUS)P_INTG# (1394)P_INTF# (CARD READER)P_INTG#	REQ1# / GNT1#
LAN	AD23	P_INTE#	REQ2# / GNT2#
Blue Thumb	AD24		

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Title

ITP

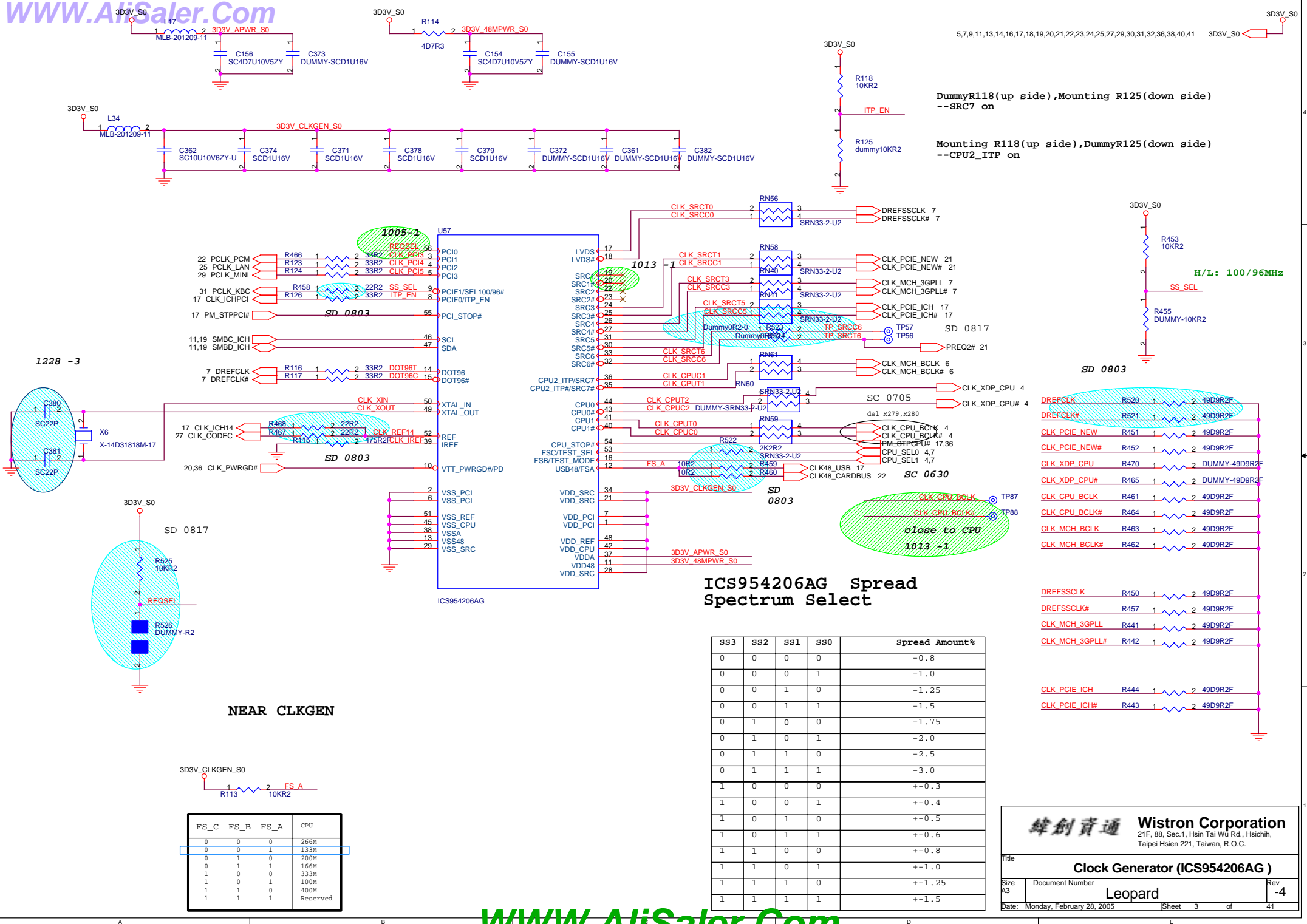
Size A3

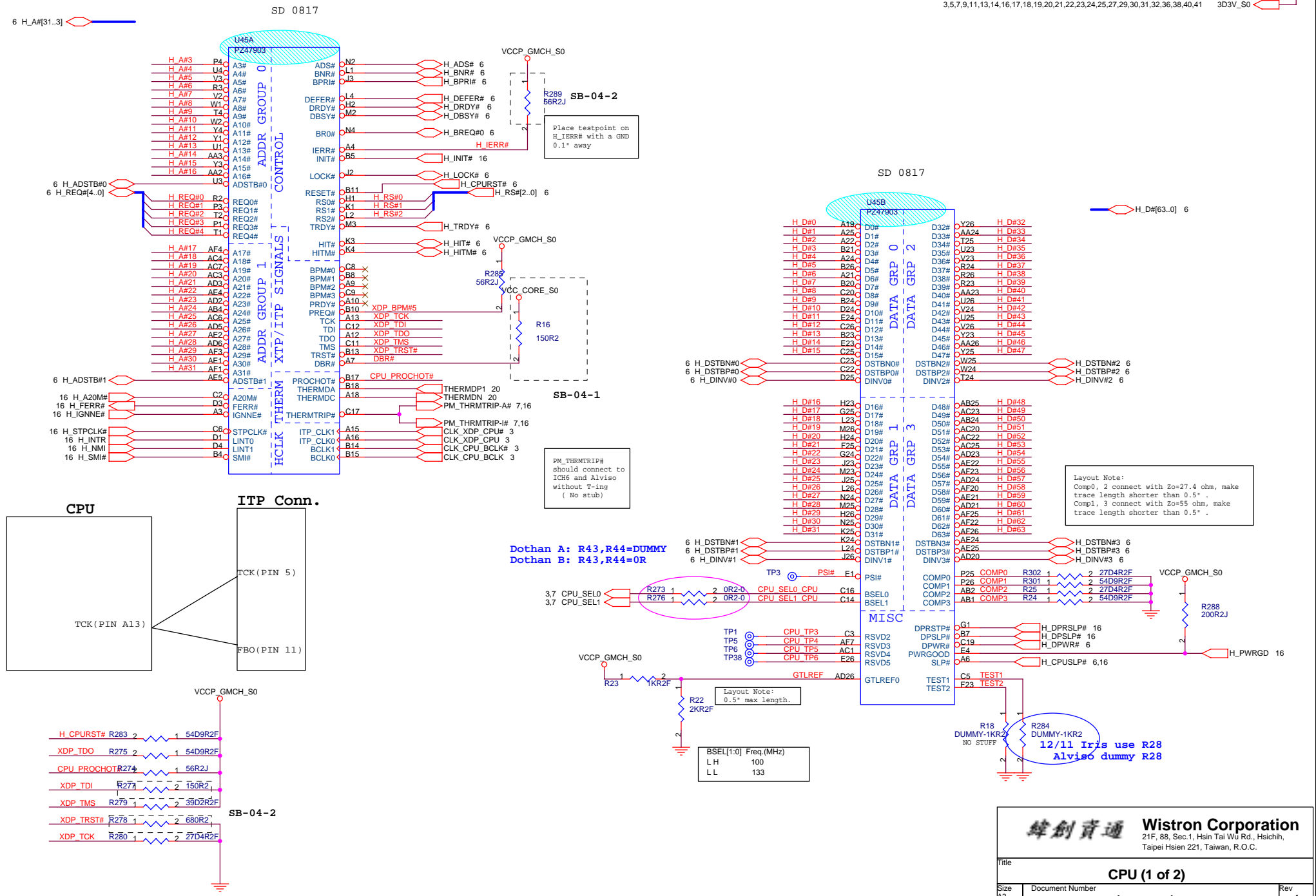
Document Number

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Date: Sunday, February 27, 2005

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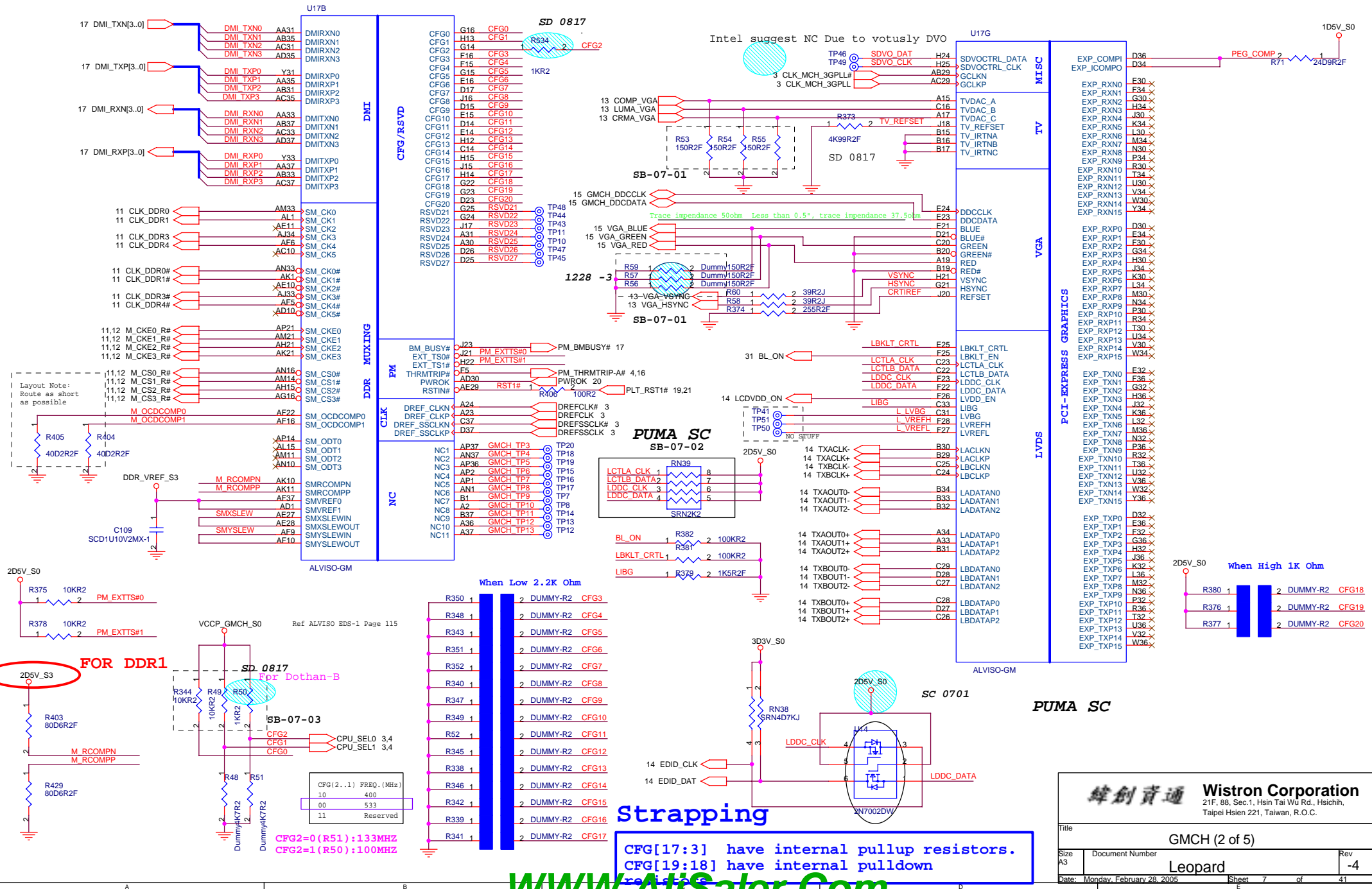




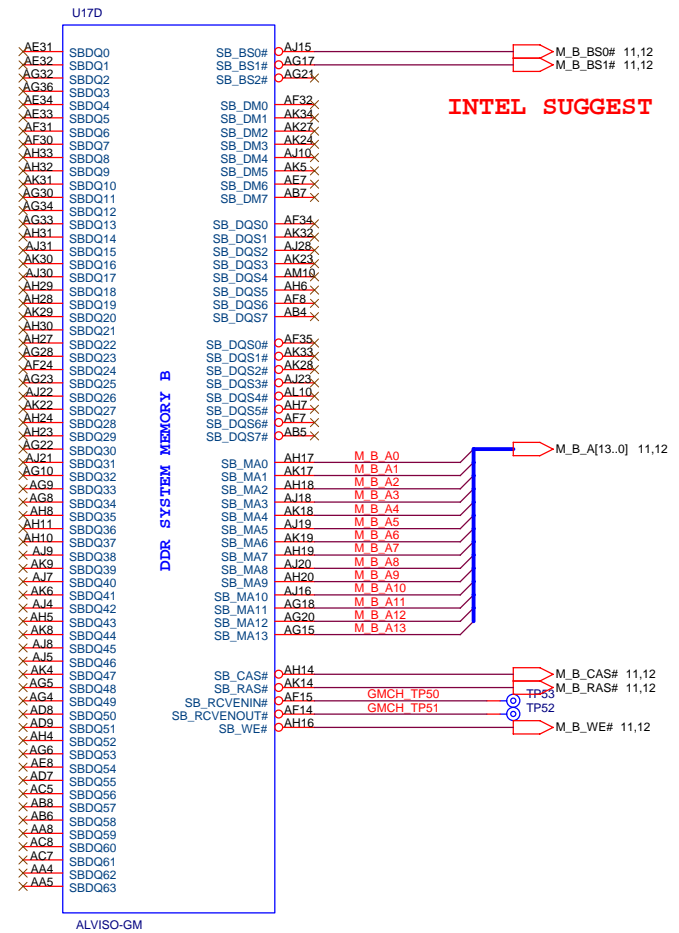
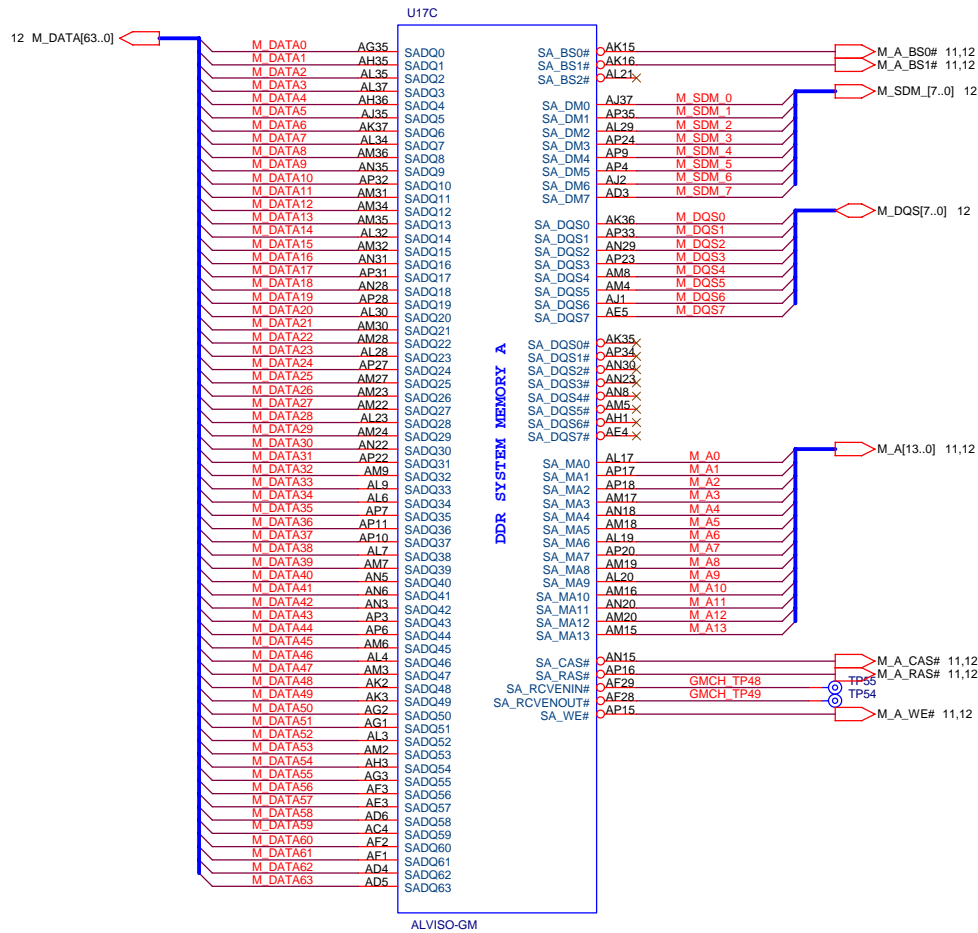
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

Alviso will provide SDVO_CTRLCLK and CTRLDATA pull downs on-die

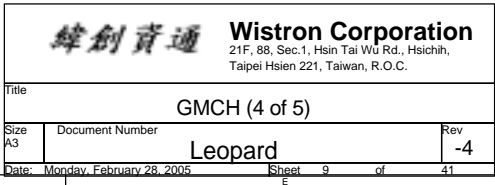
9,15,18,40 2D5V_S0
9,10,11,12,38,39,40,41 2D5V_S3
5,9,17,18,21,38,39,41 1D5V_S0
6,9,10,40,41 CORE_GMCH_S0
11,40 DDR_VREF_S3

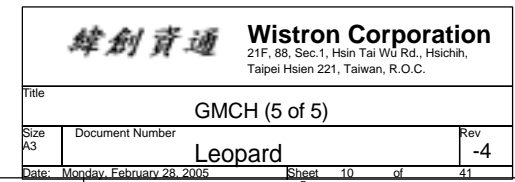


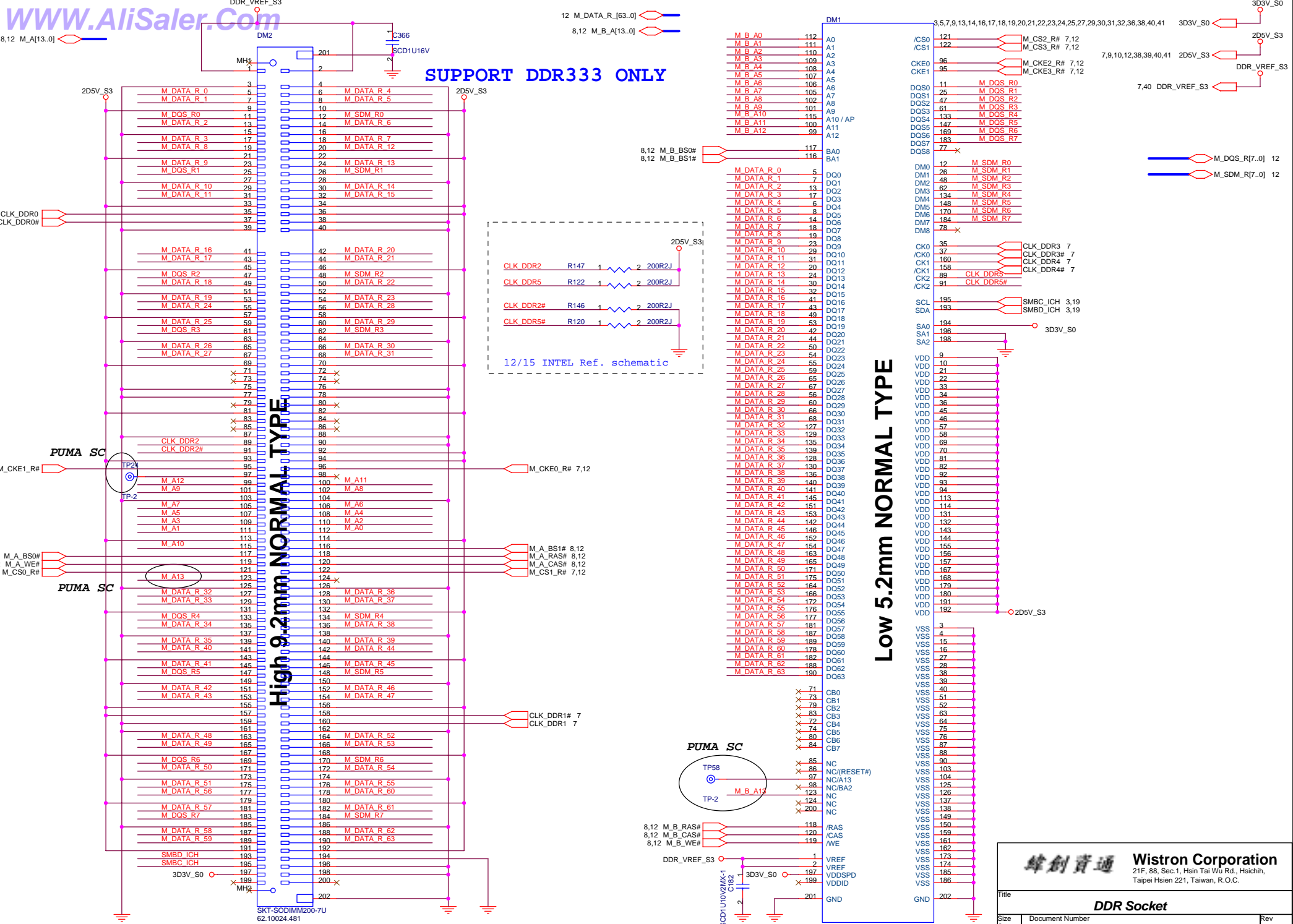
SUPPORT DDR333 ONLY



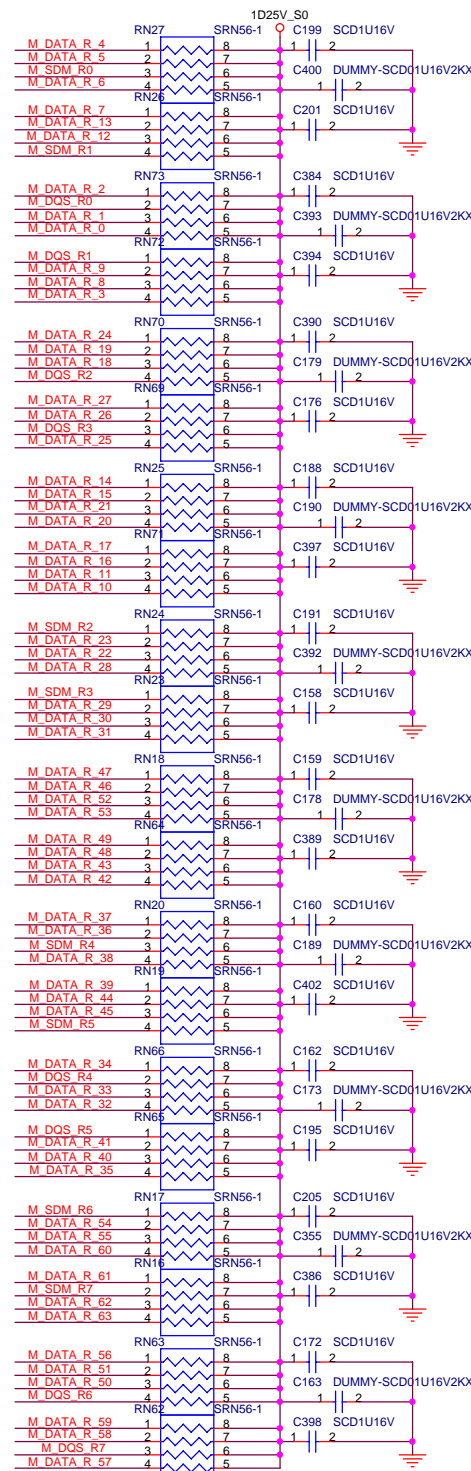
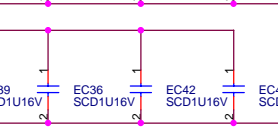
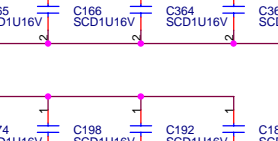
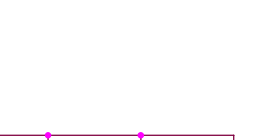
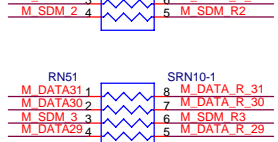
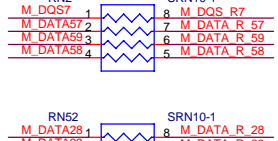
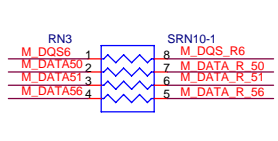
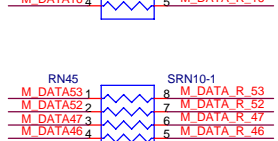
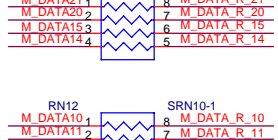
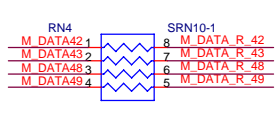
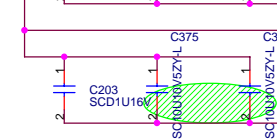
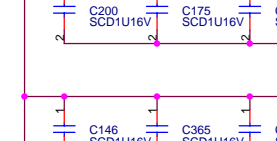
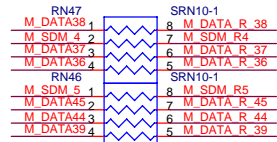
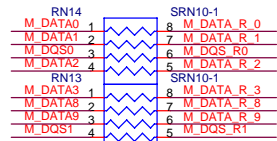
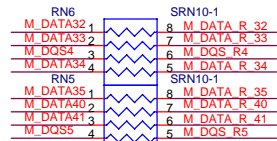
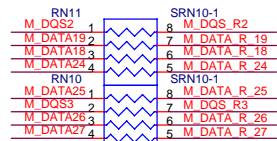
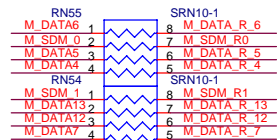
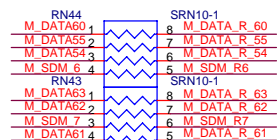
INTEL SUGGEST





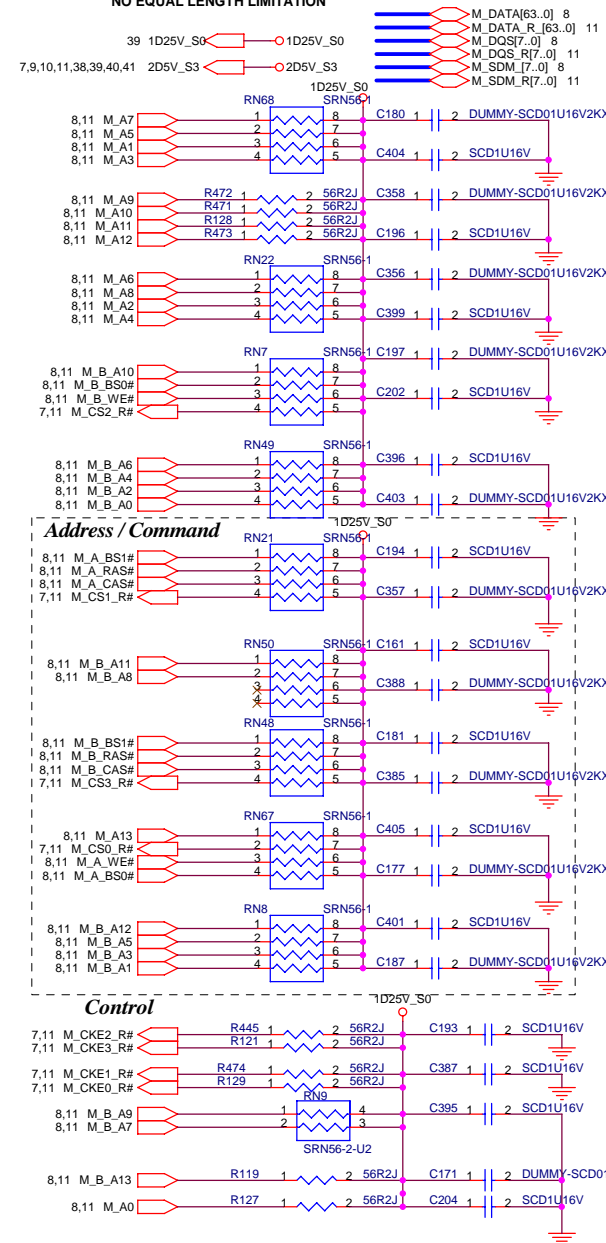


SERIES DAMPING *PUMA-SC*
Change RN to small size



PARALLEL TERMINATION

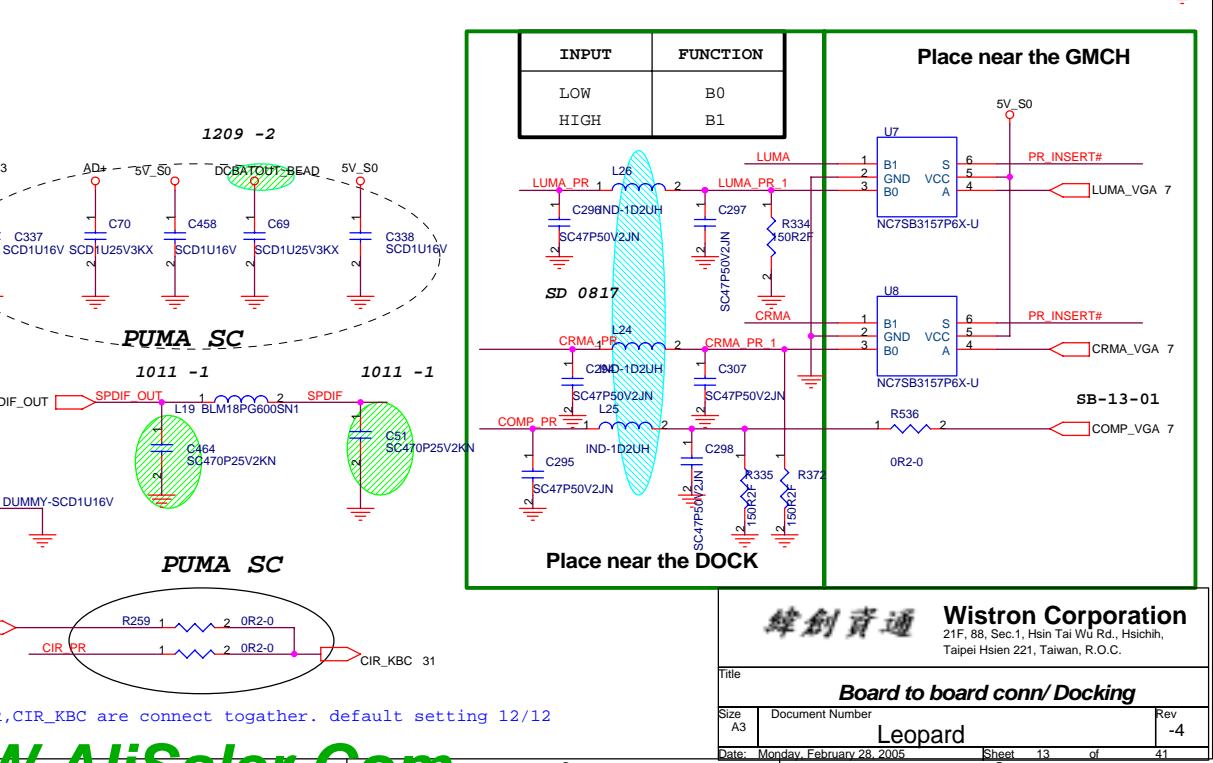
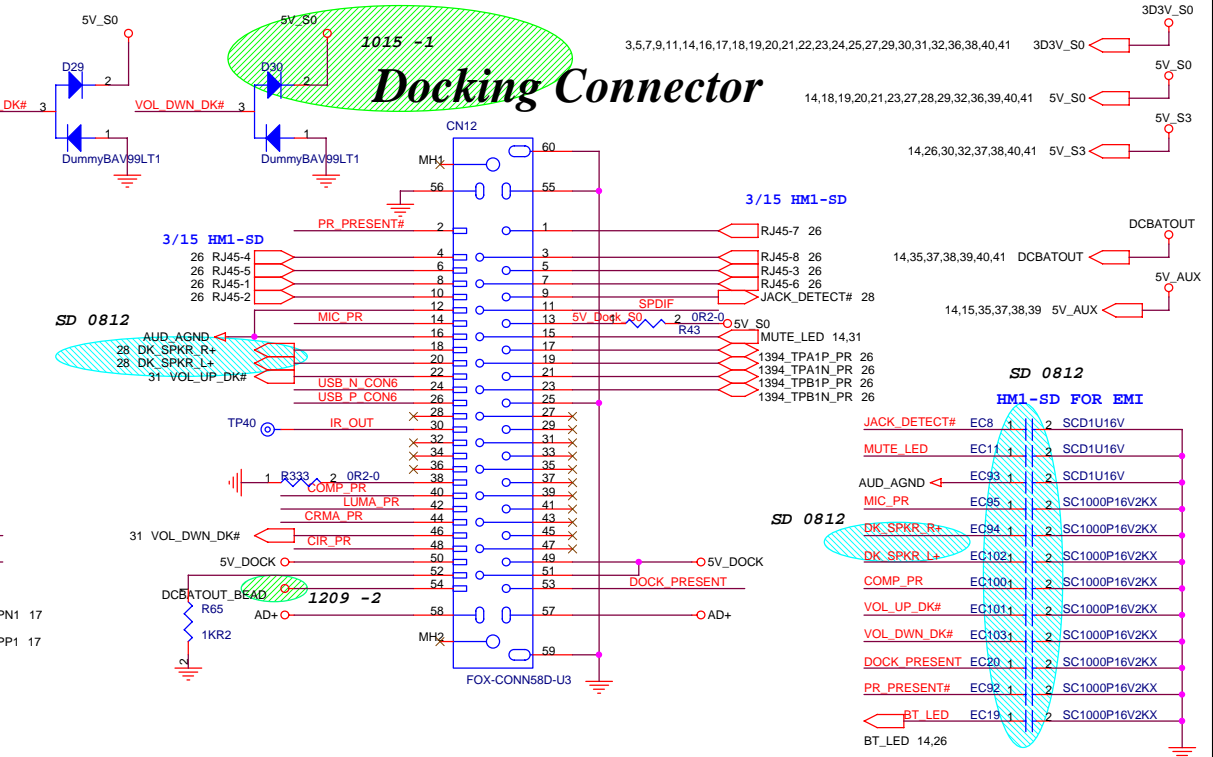
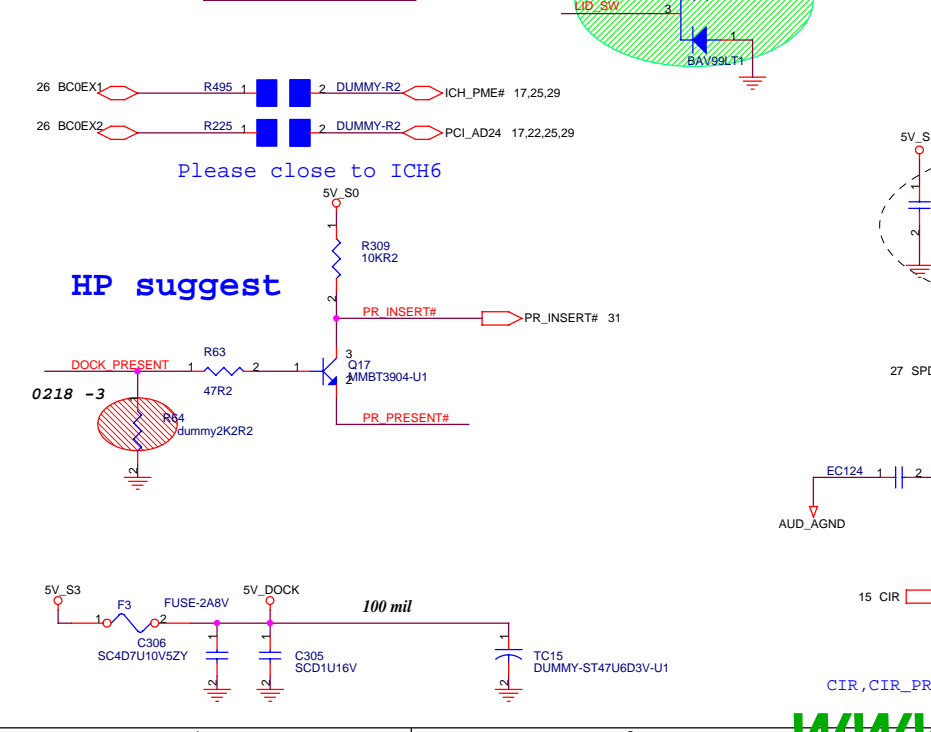
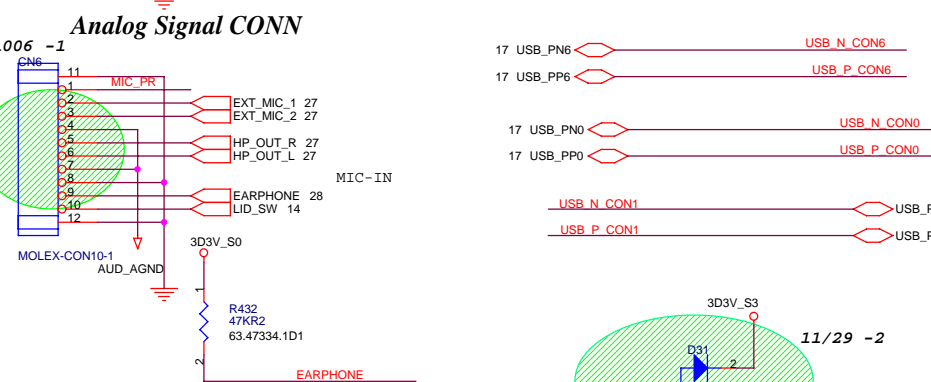
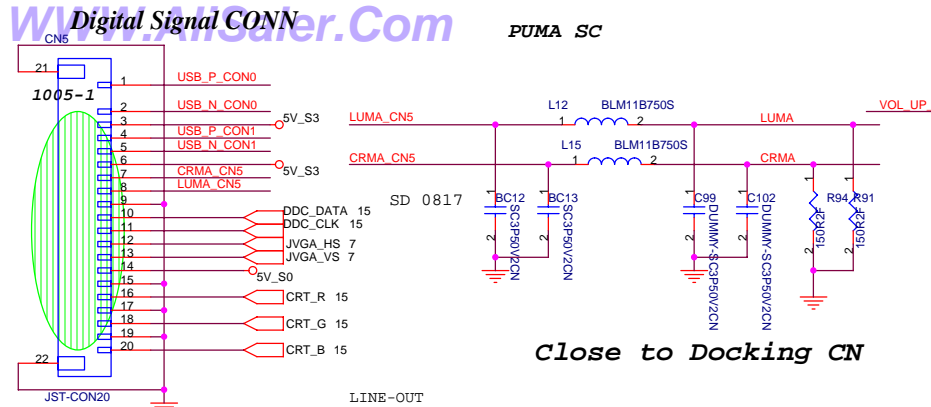
**PULL HIGH STUBS $< 0.8"$, PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION**



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Taipei Hsien 221, Taiwan, R.O.C.

DDR Serial/Terminator Resistor

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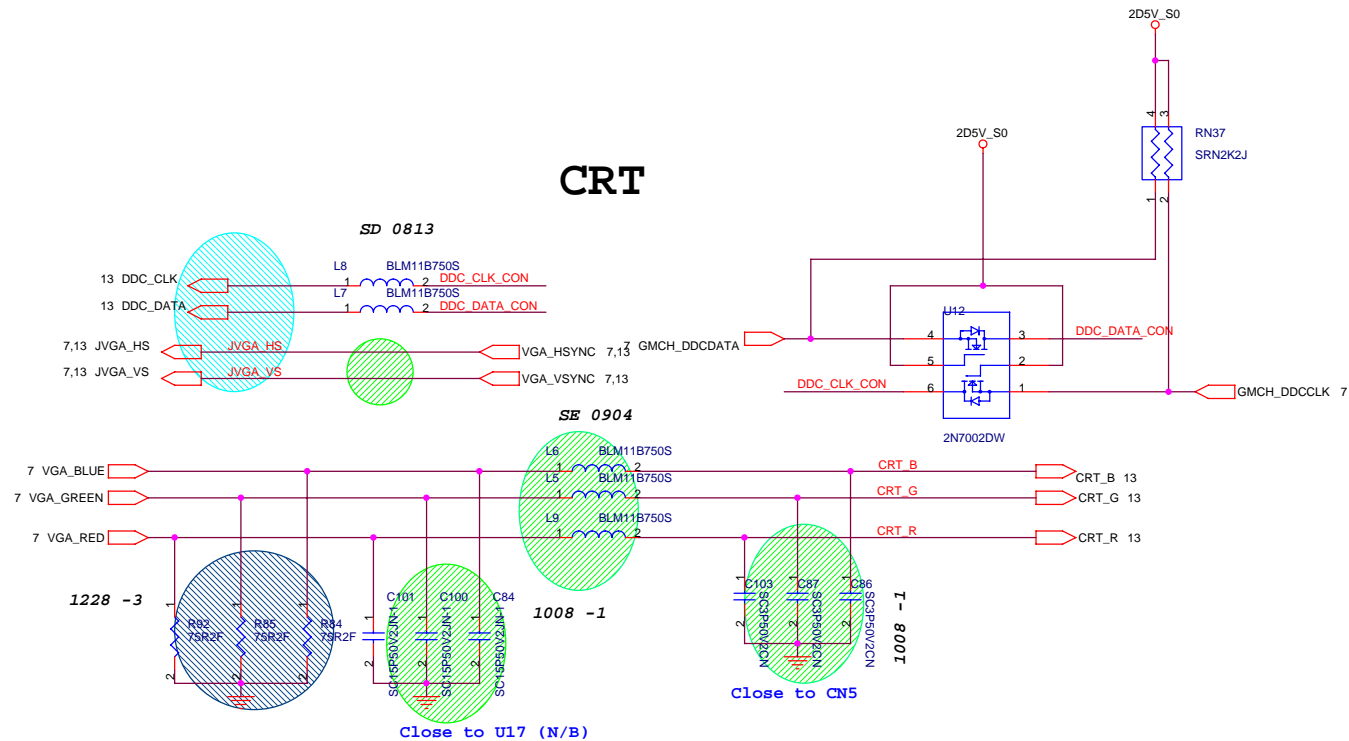




PA & PR diffent parts

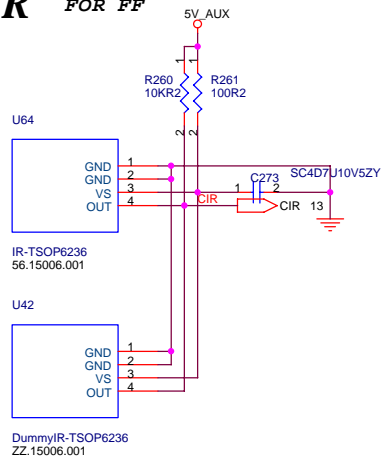
	PA	PR
LED1	83.00190.Y70	83.00190.W70
LED2	83.00190.Y70	83.00190.W70
LED4	Dummy	83.00110.D70
LED5	Dummy	83.00110.D70
LED6	Dummy	83.00110.D70
LED7	83.00110.E70	Dummy
LED8	83.00110.E70	Dummy
LED9	83.00110.E70	Dummy
U64	56.15006.001	Dummy
U42	Dummy	56.15006.001
R256	63.20134.1D1	63.12234.1D1
R257	63.20134.1D1	63.12234.1D1
R258	63.20134.1D1	63.12234.1D1
R93	63.20134.1D1	63.12234.1D1
R112	63.20134.1D1	63.12234.1D1

CBUS1	21.H0088.001	21.H0088.001
R176	63.10334.1D1	Dummy
R177	Dummy	63.10334.1D1

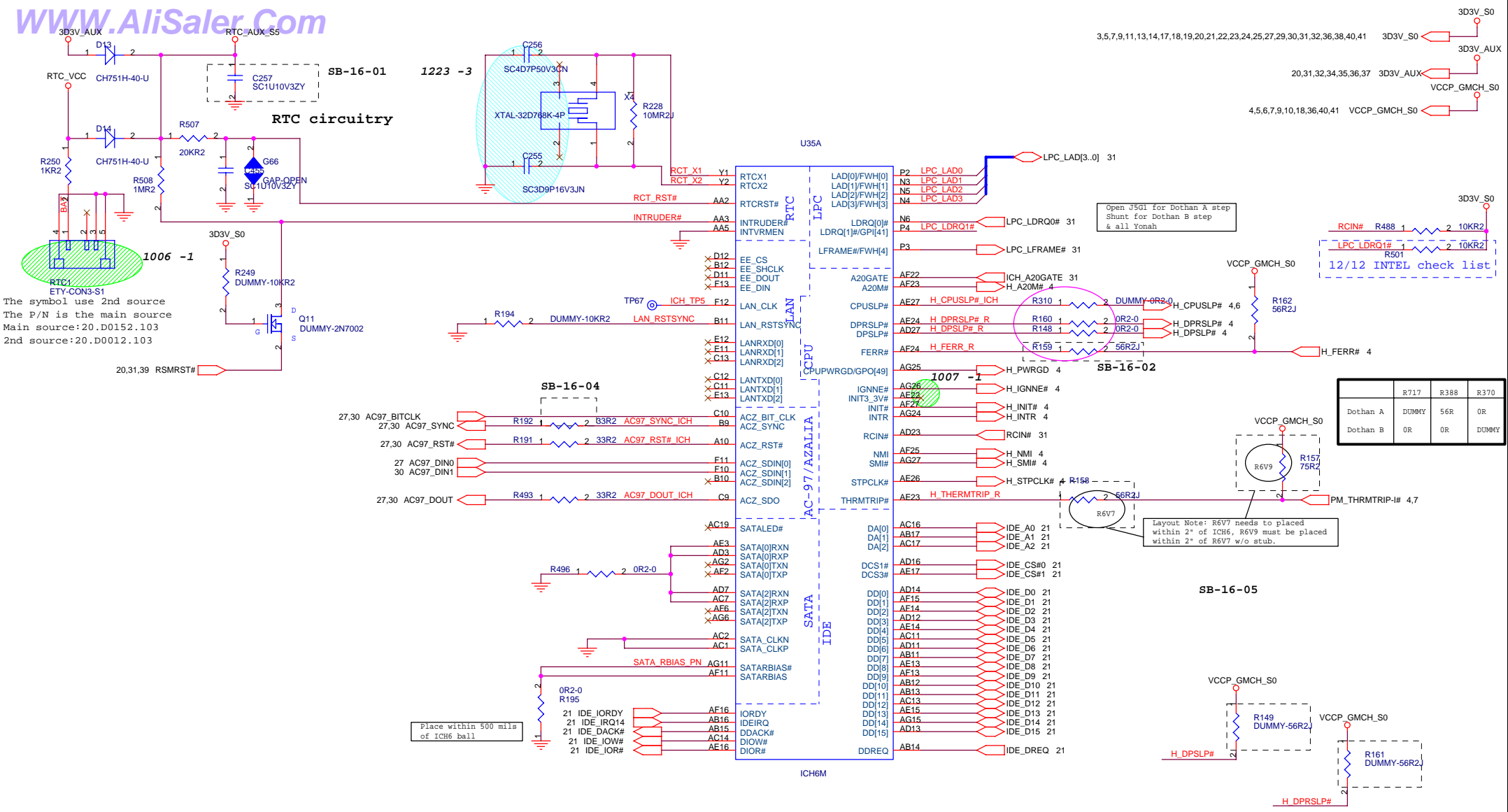


010804 Modified on Astro ID request

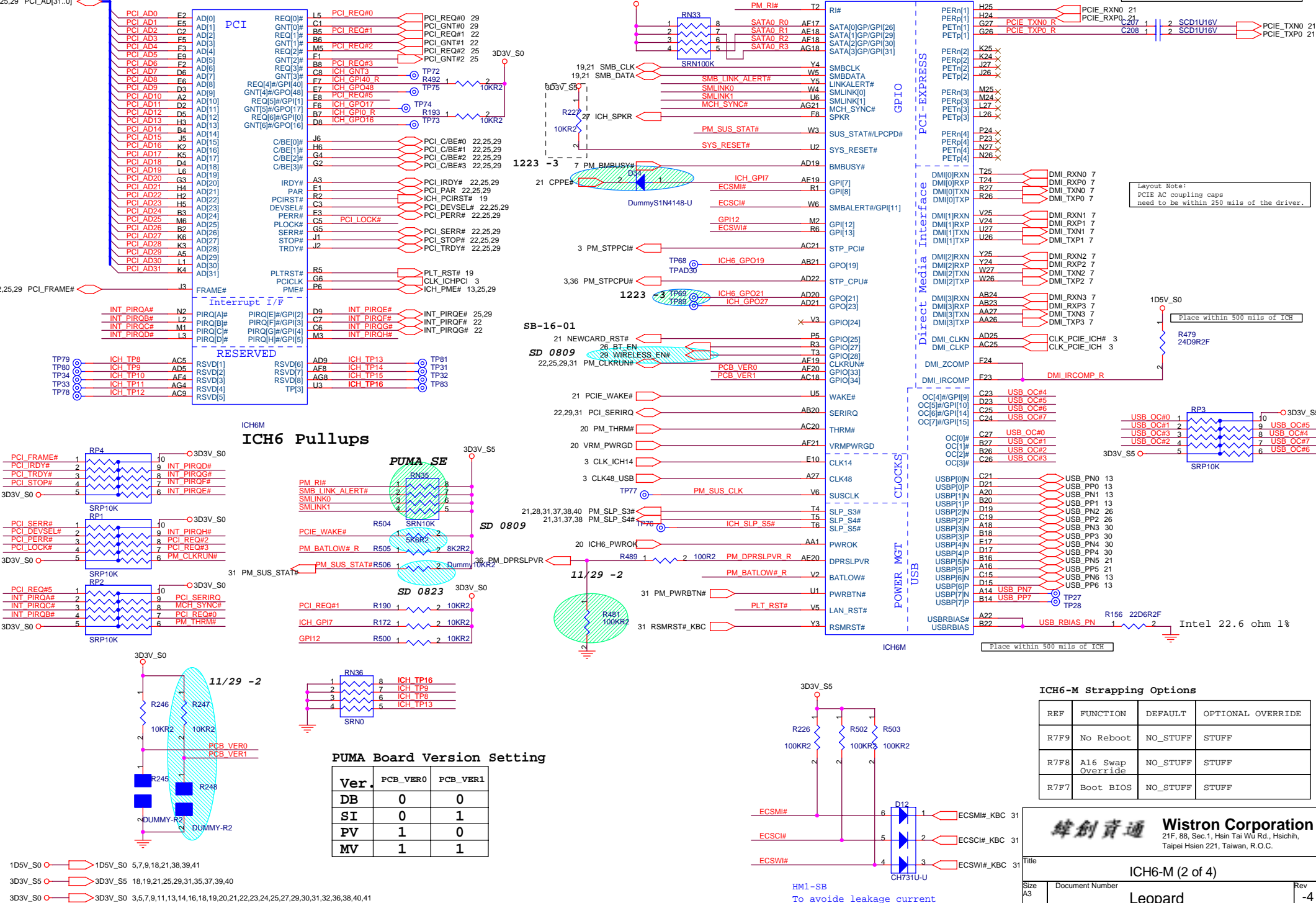
CIR FOR FF

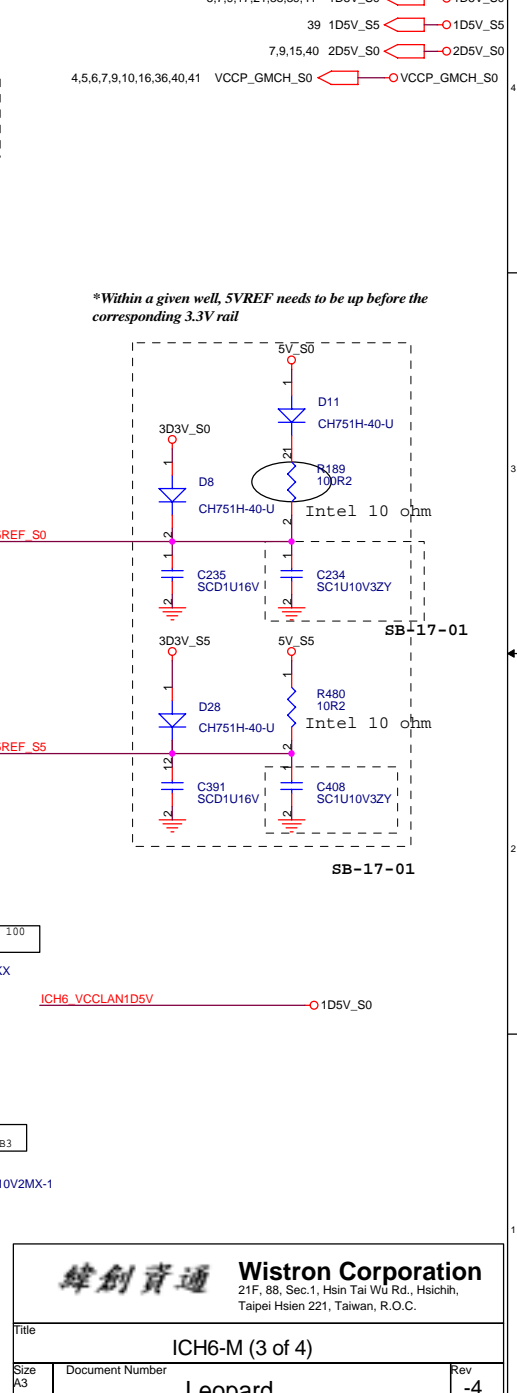
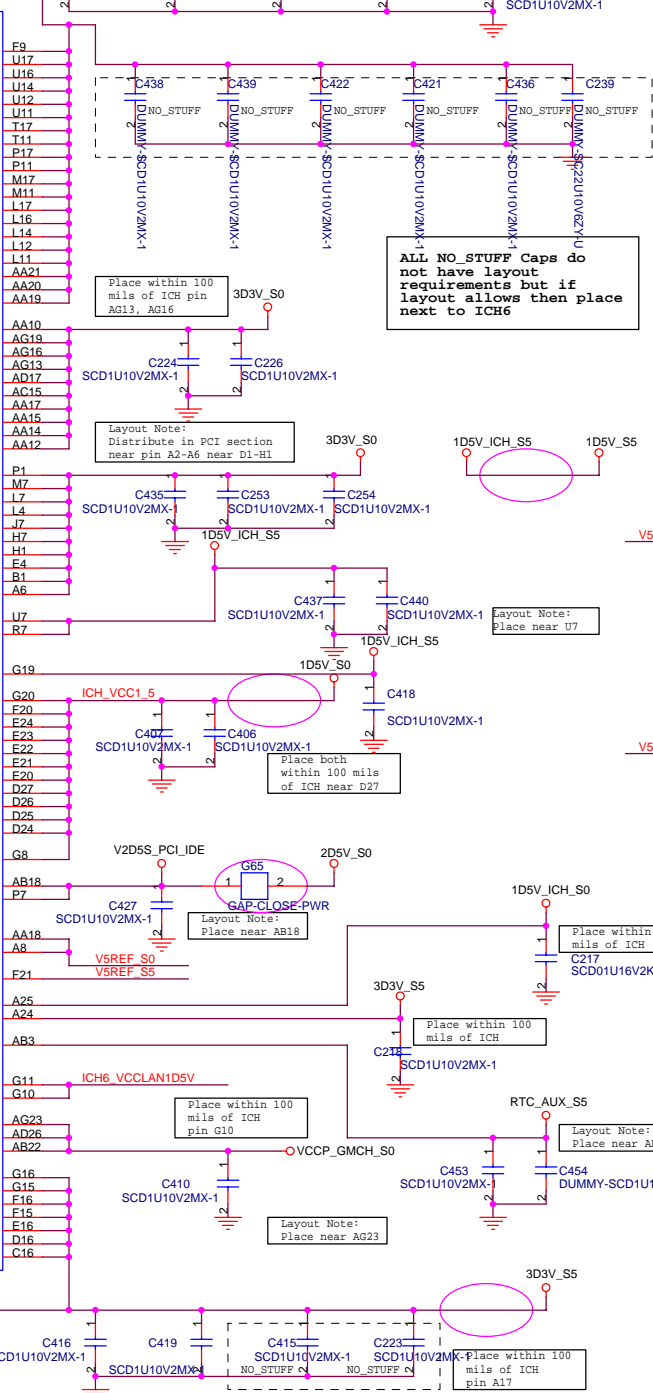
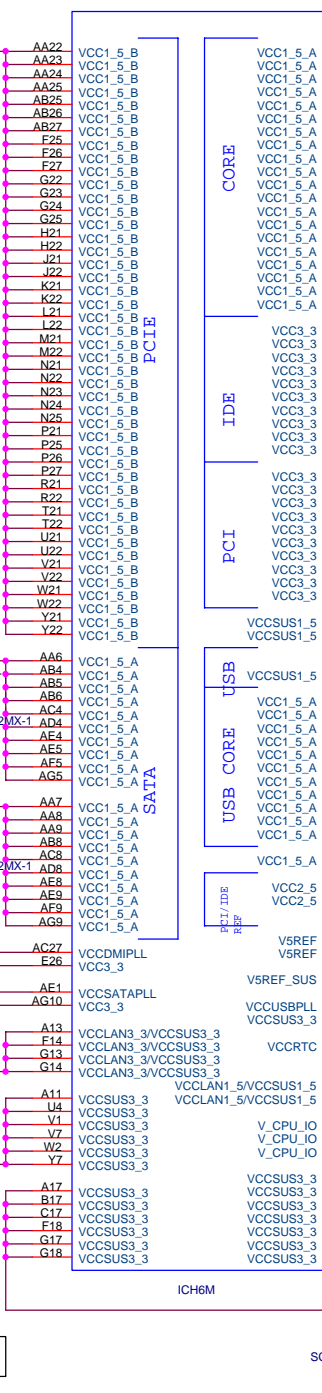
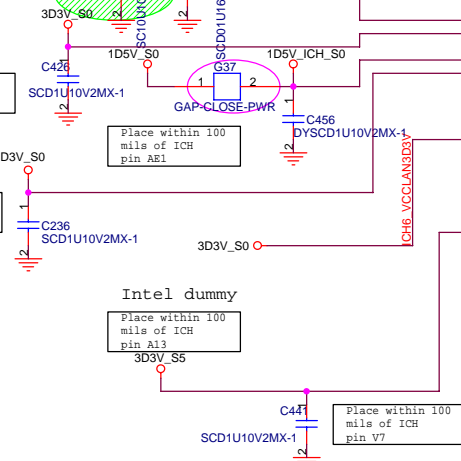
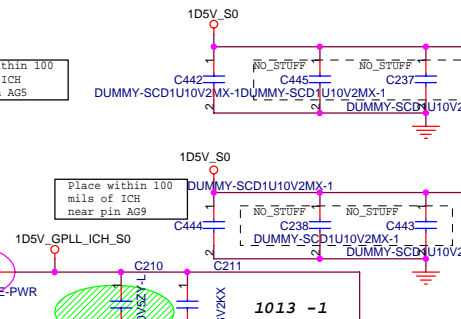
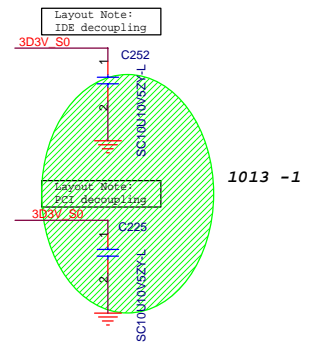


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Title CRT/ CIR	
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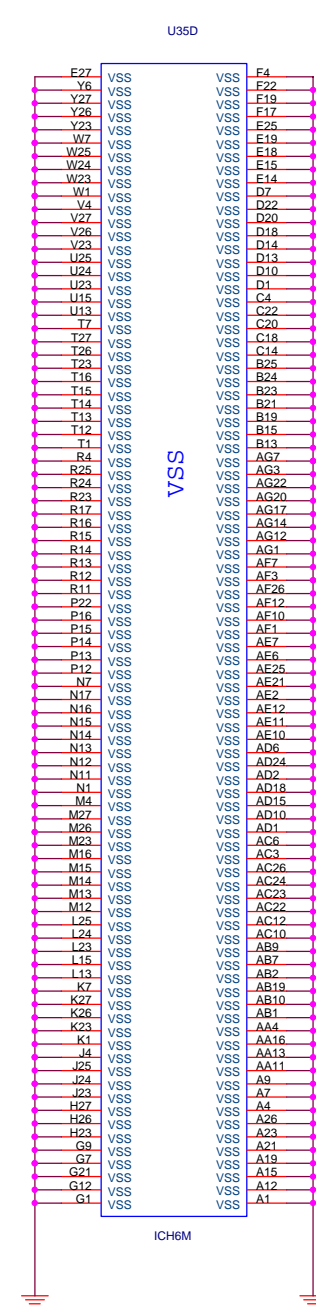
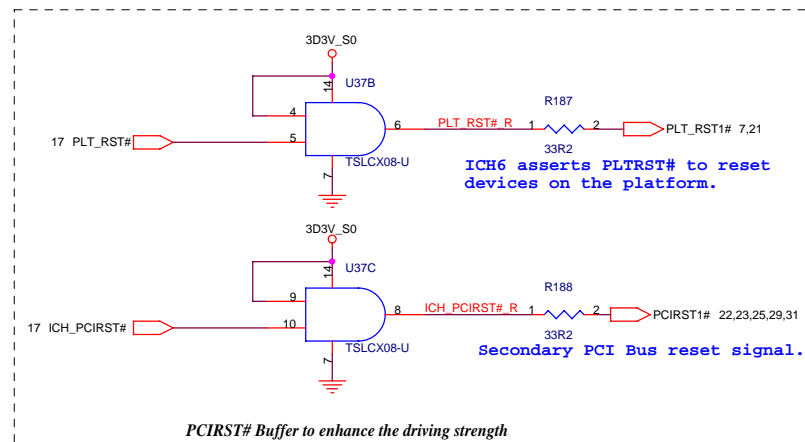
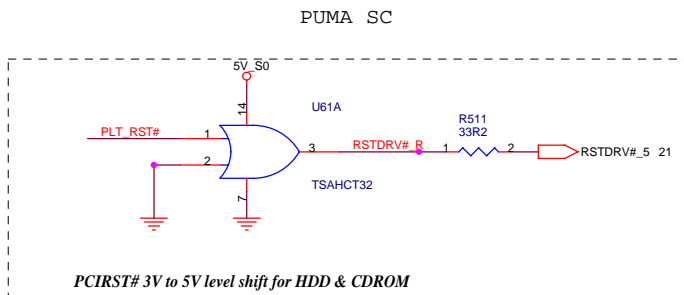
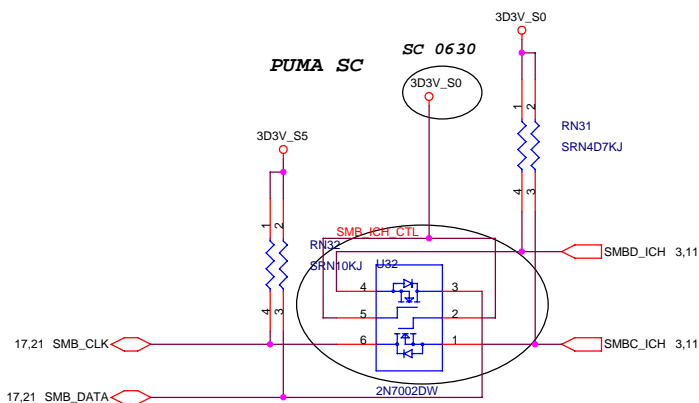


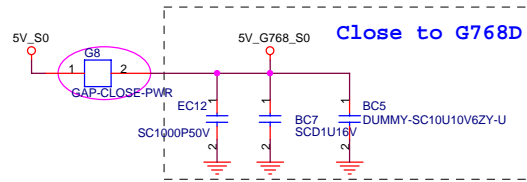
	R717	R388	R370
Dothan A	DUMMY	56R	OR
Dothan B	OR	OR	DUMMY



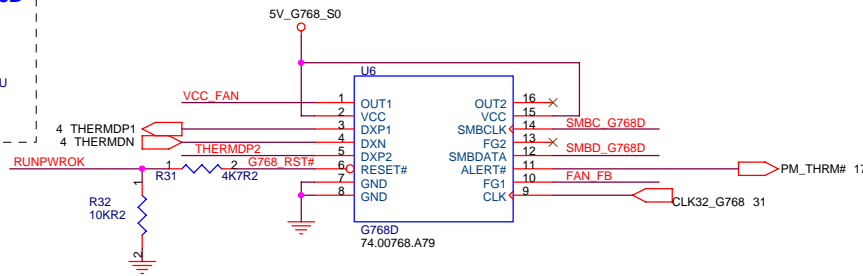


SMBUS (ICH6 ---> SODIMM,CLKGEN)

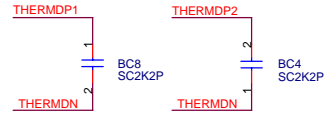
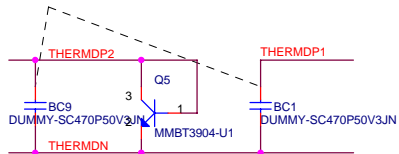




Reserve for G768B
works at High
Speed

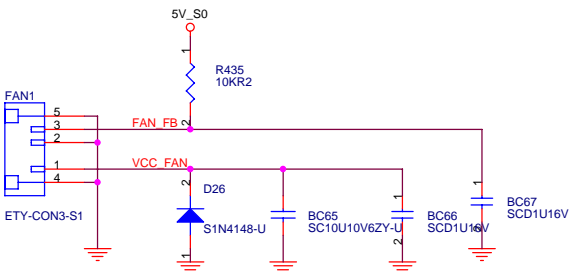


Put these two Caps near the thermal diode.



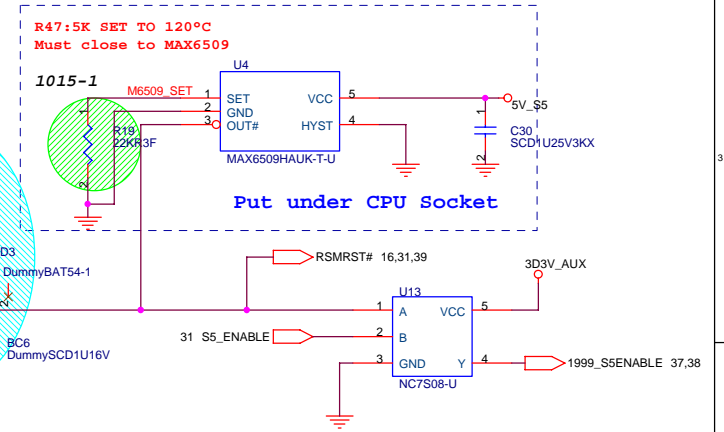
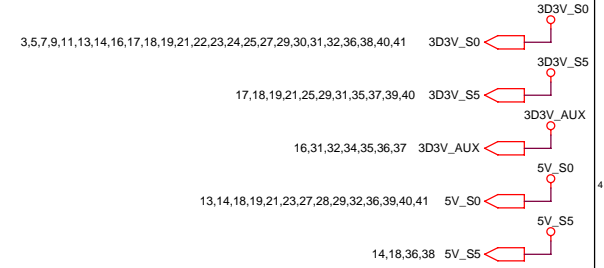
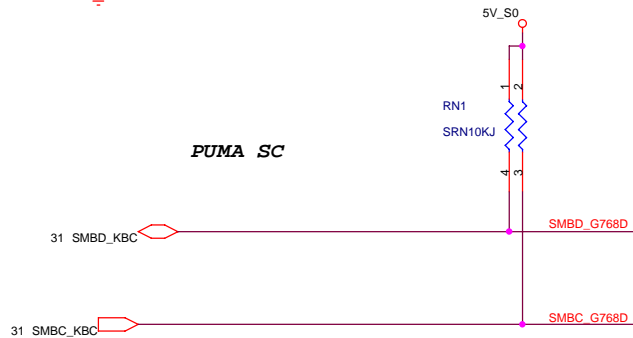
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B

180 ms after VCC_G768 > 4.38v, p2, 7



The symbol use 2nd source
The P/N is the main source
Main source:20.D0152.103
2nd source:20.D0012.103

PUMA SC

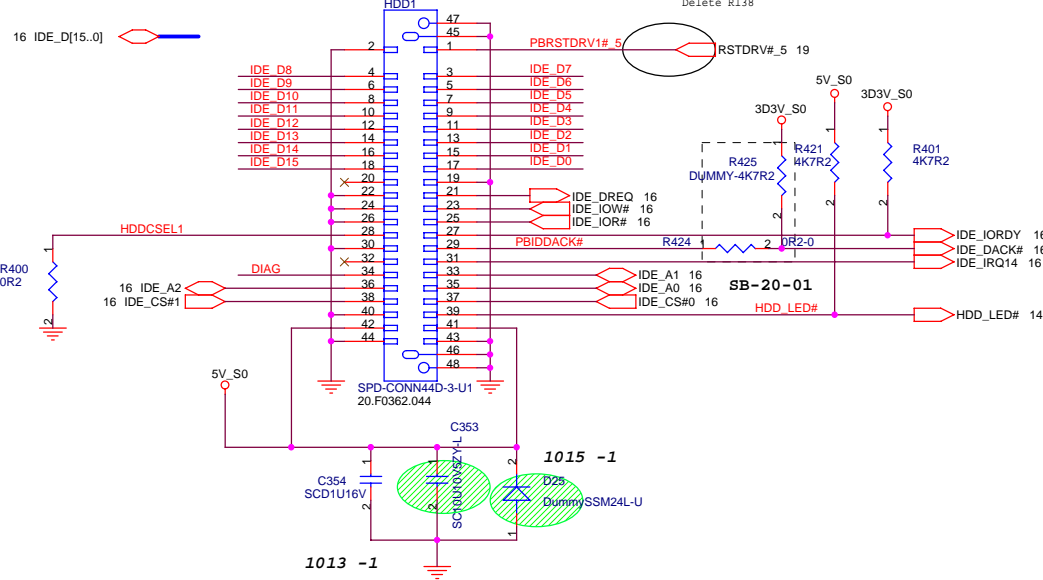


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Taipei Hsien 221, Taiwan, R.O.C.

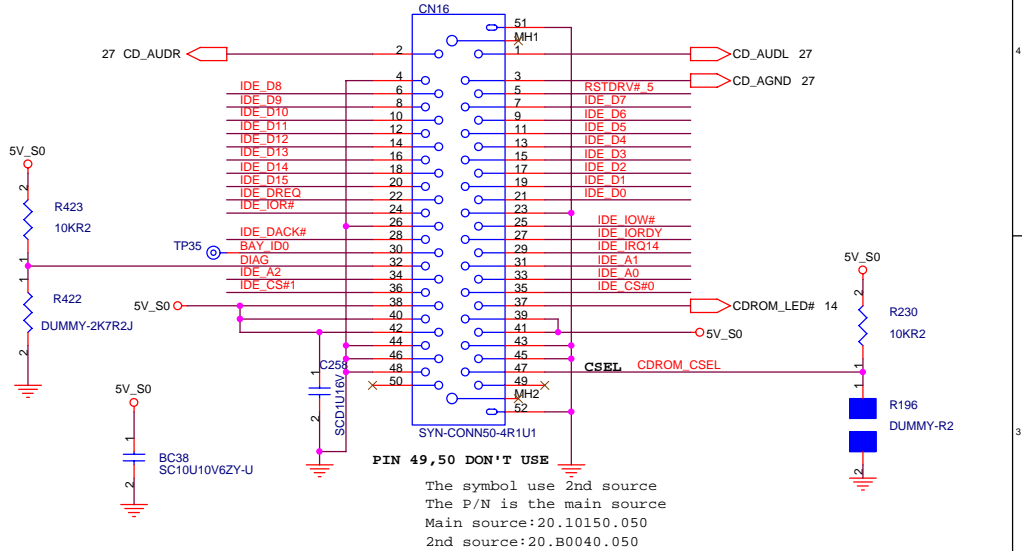
Title			G768D	
Size	Document Number	Leopard		Rev
A3				-4
Date:	Monday, February 28, 2005	Sheet	20	of 41

HDD Connector

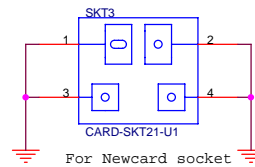
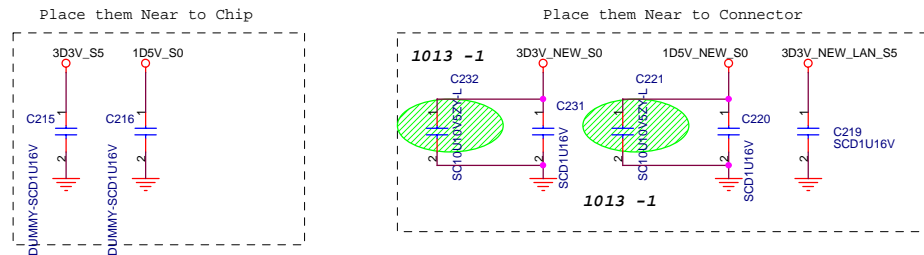
SC 0712
Delete R138



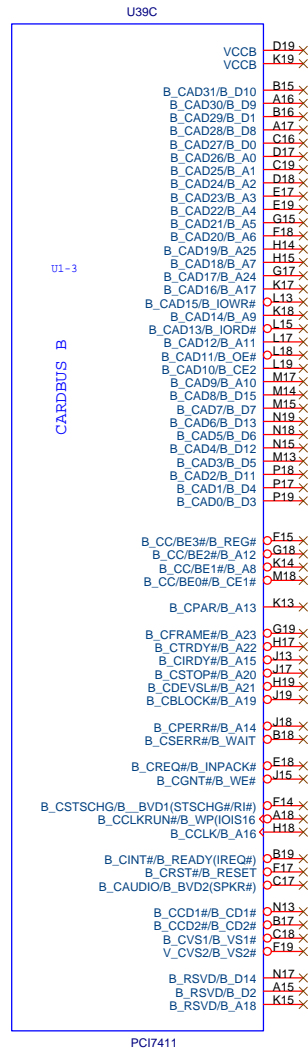
CDROM

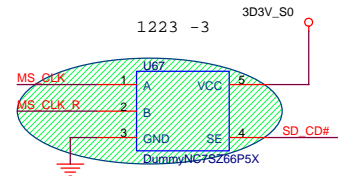
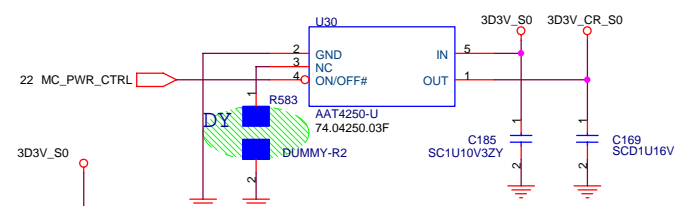
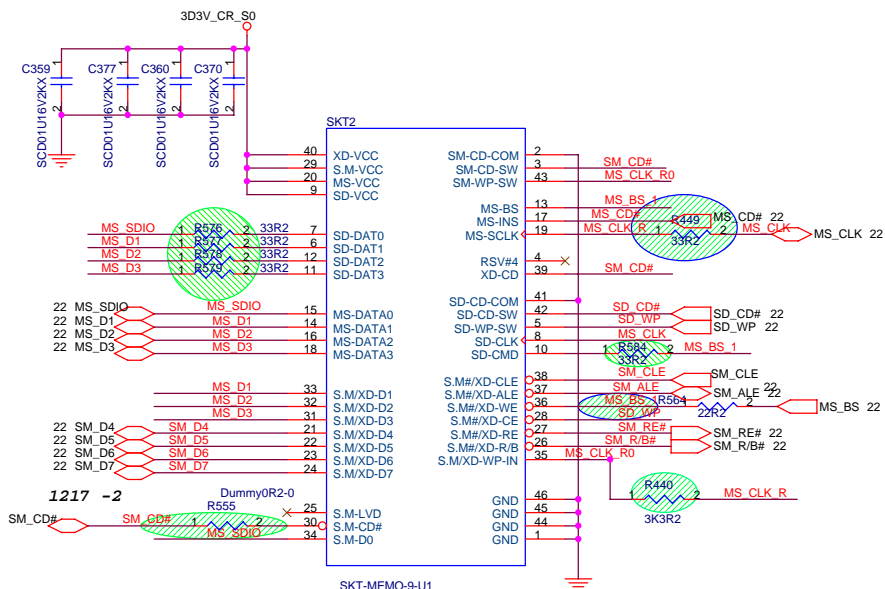
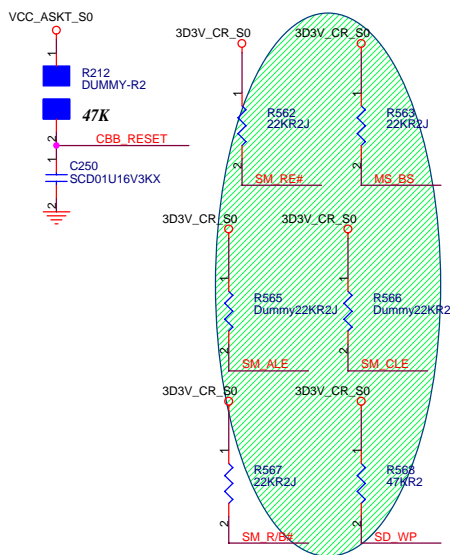
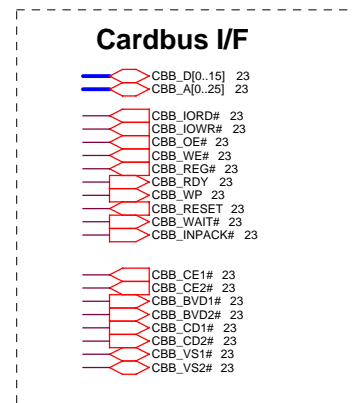


NEWCARD Connector









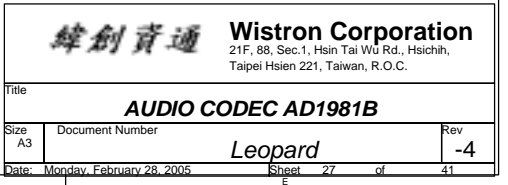
6 in 1 Connector

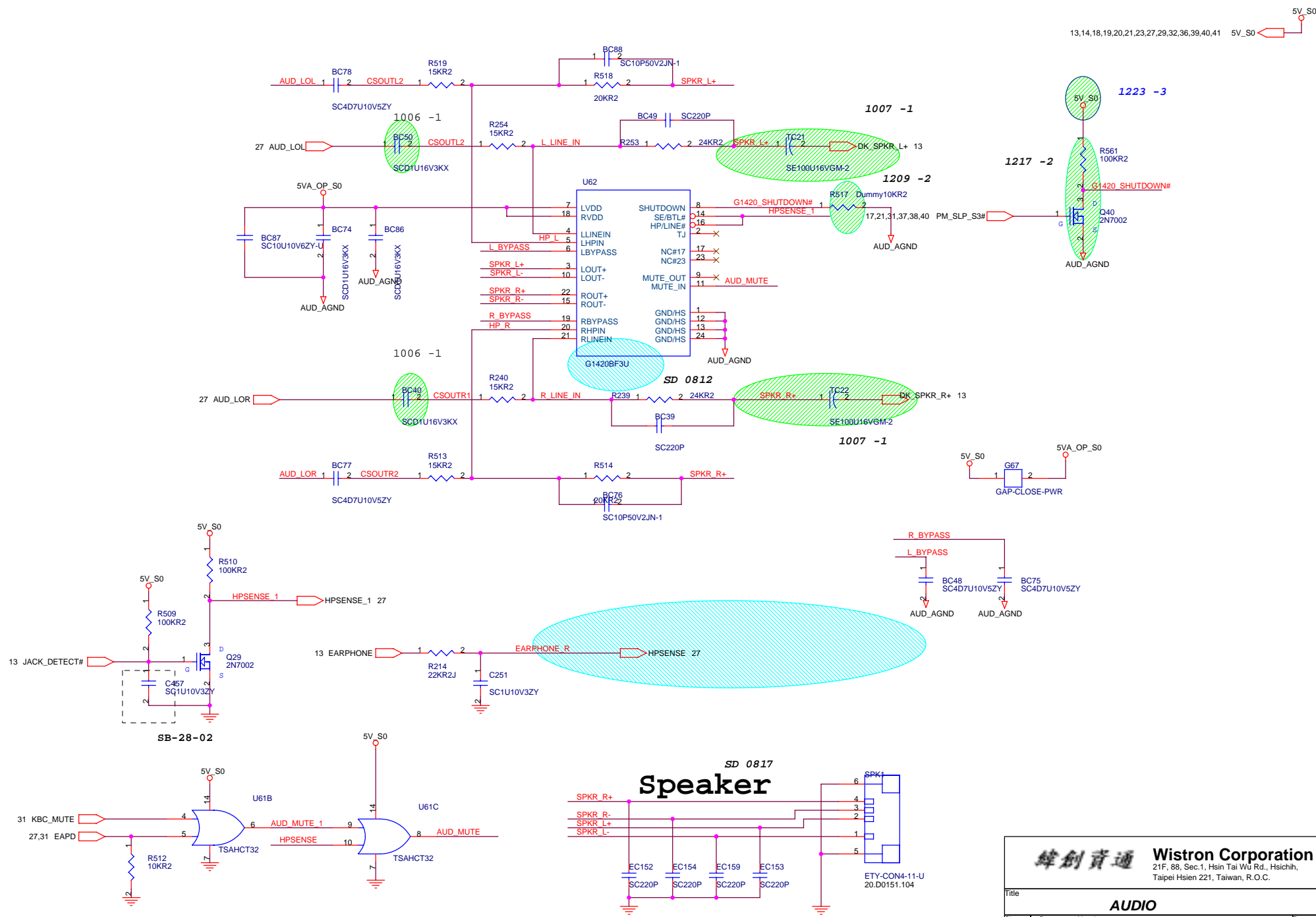


SC 0708

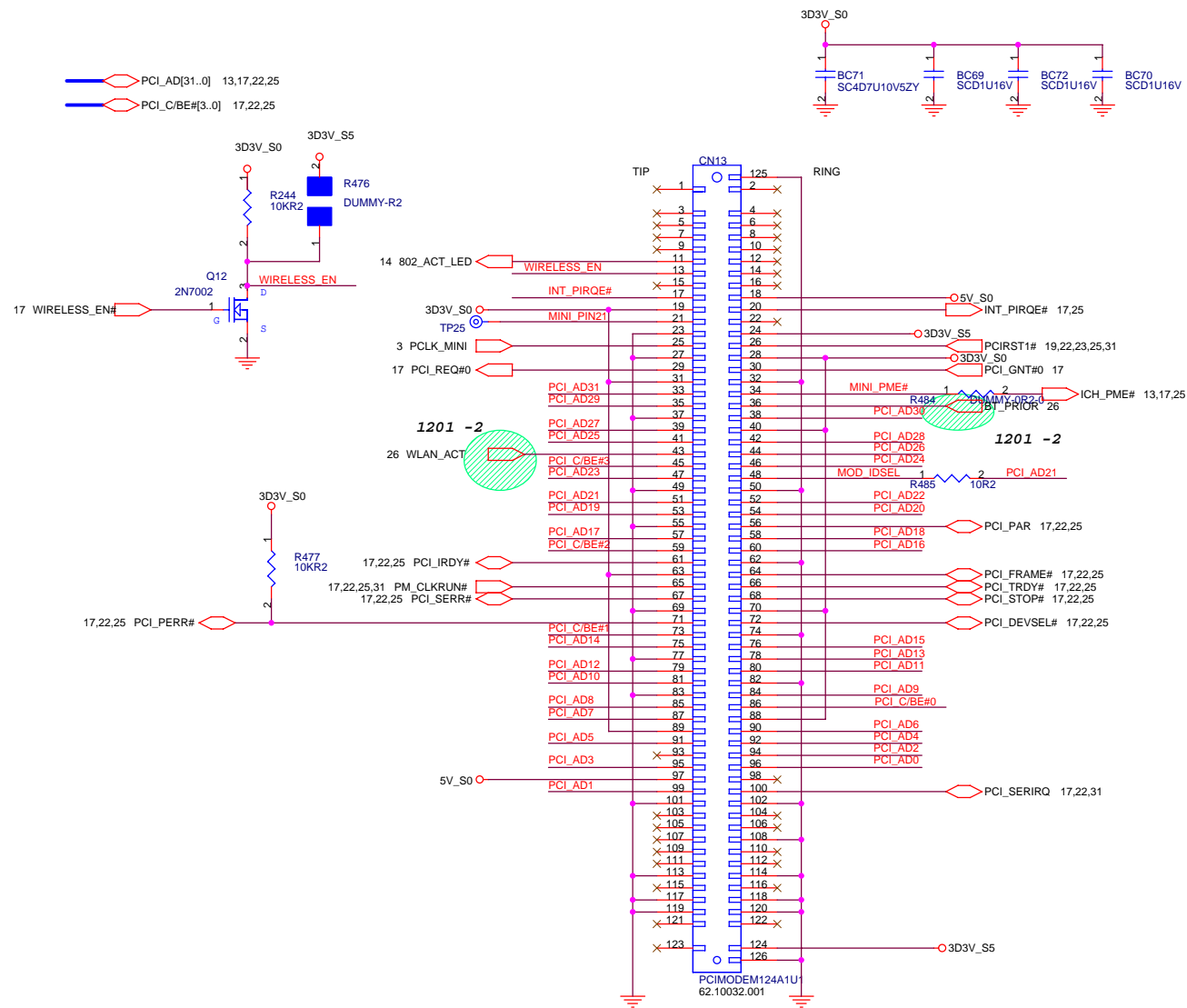








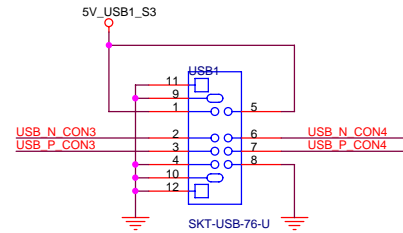
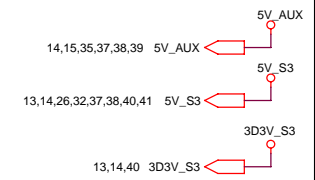
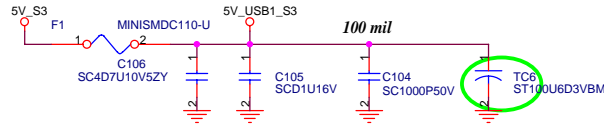
MINI-PCI



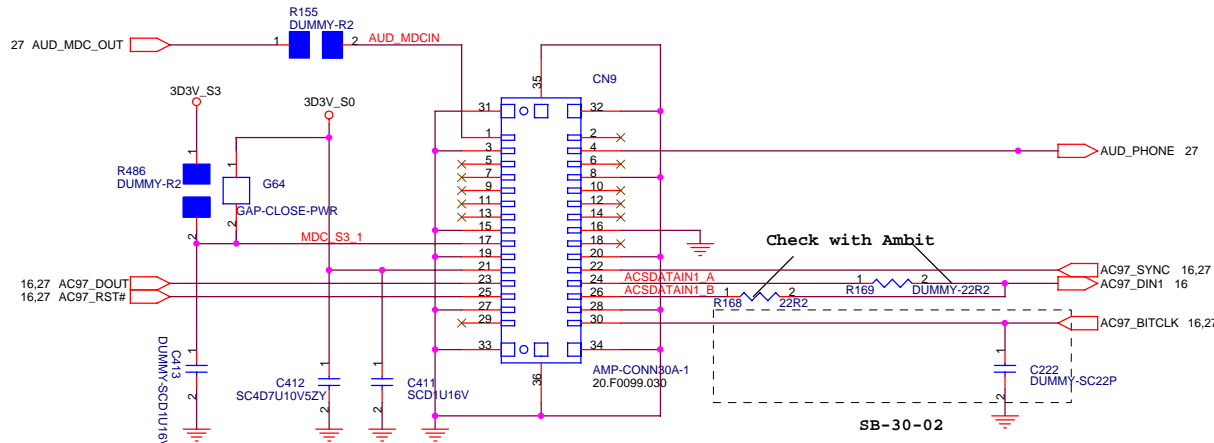
The symbol use 2nd source
 The P/N is the main source
 Main source: 62.10032.001
 2nd source: 62.10032.031

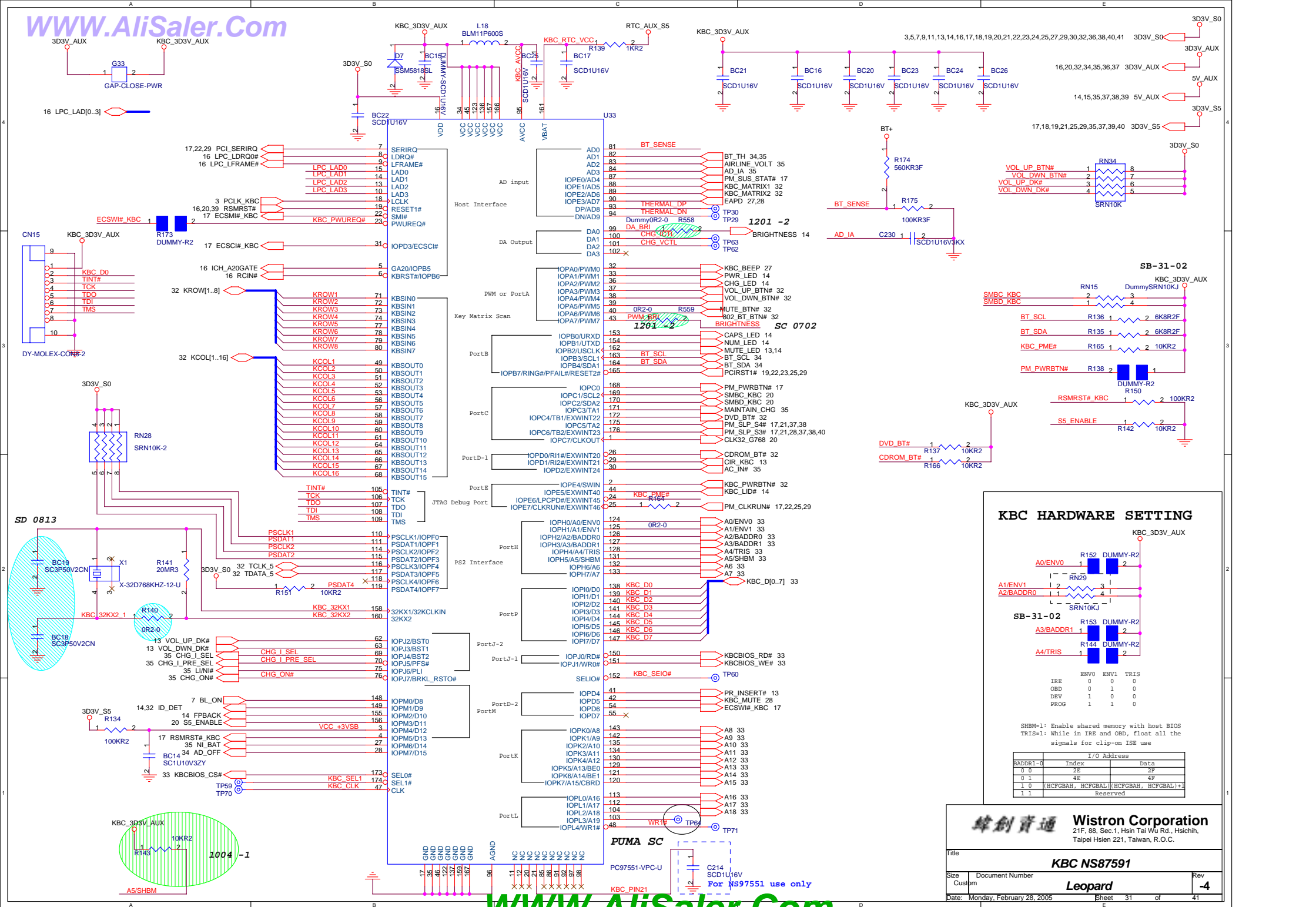
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI-PCI	
Size: A3	Document Number: Leopard
Date: Monday, February 28, 2005	Sheet: 29 of 41
Rev: -4	

USB POWER



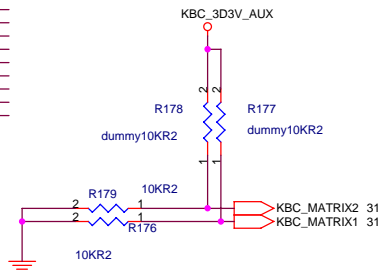
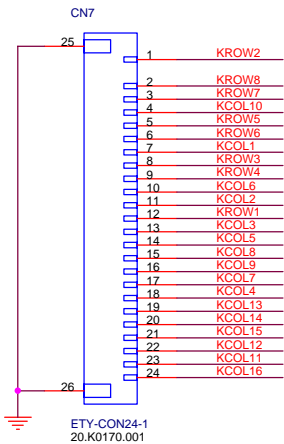
MDC Connector





INTERNAL KEYBOARD CONNECTOR

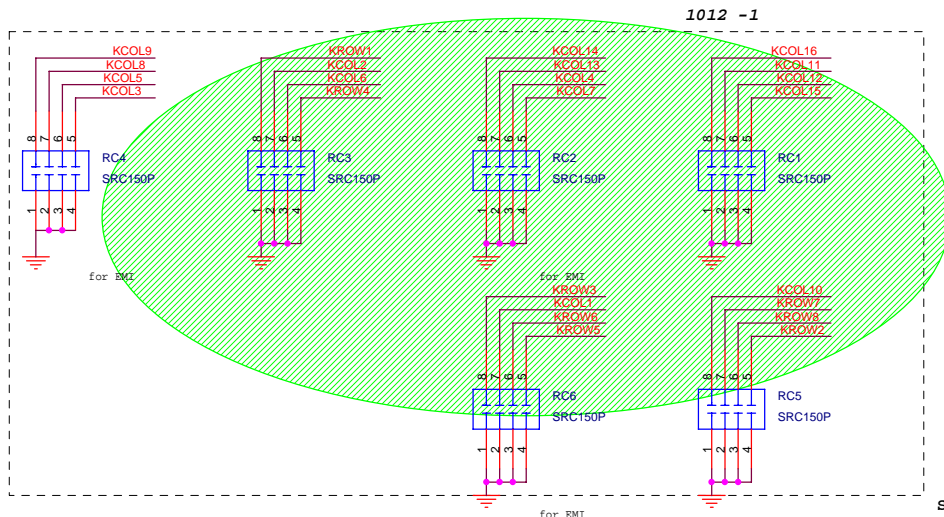
KROW[1..8] 31 KCOL[1..16] 31



the matrix table for PCB

KBC_MATRIX2, KBC_MATRIX1	PA	PR
FF	00	01
DF	10	11

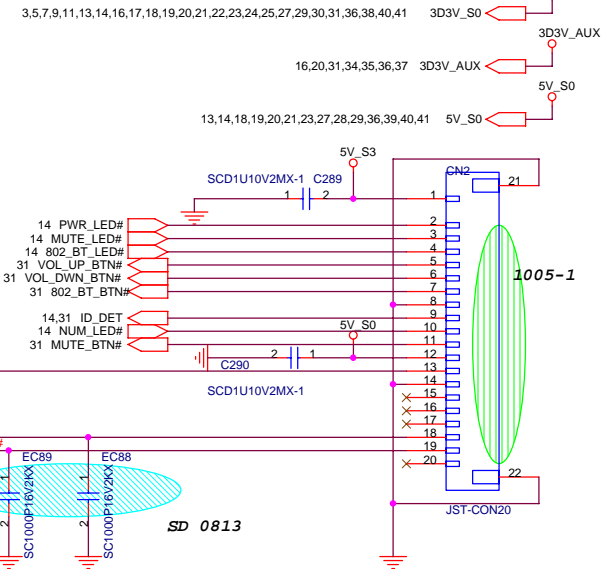
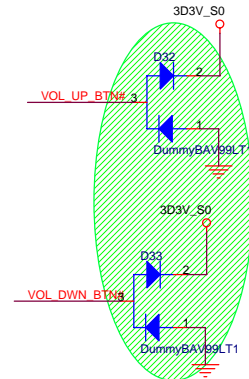
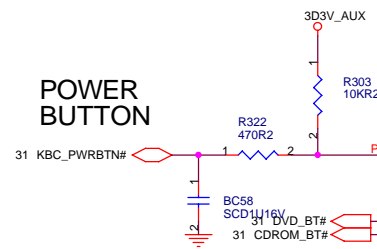
	NONE Quick Play	Quick Play
MATRIXID1#	0	1



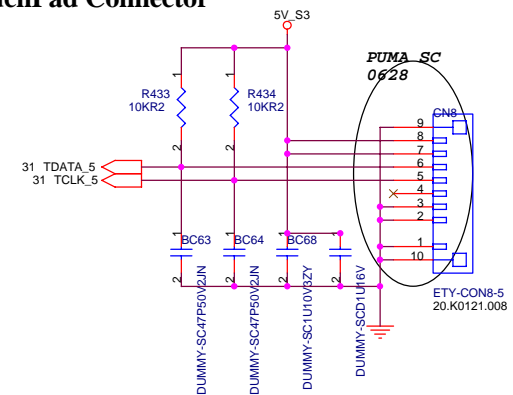
SB-32-01

LAUNCH Board

POWER BUTTON



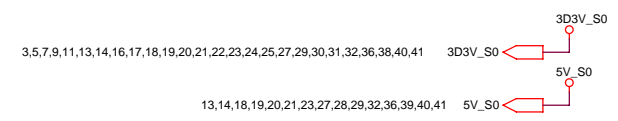
TouchPad Connector



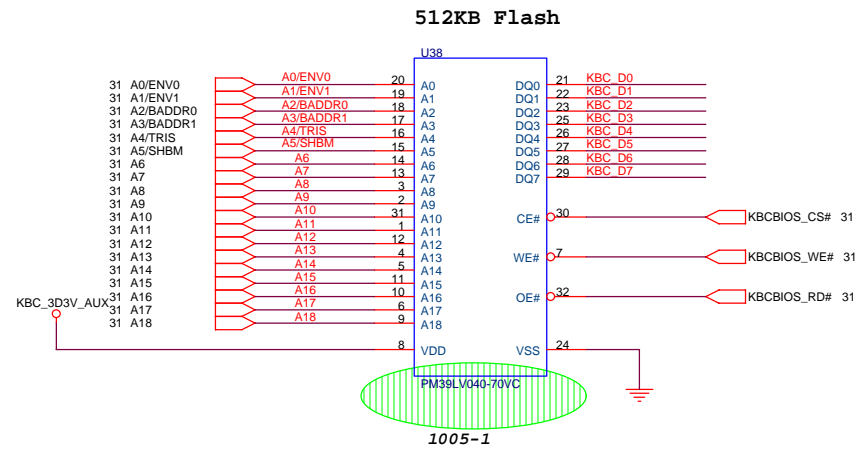
緯創資通

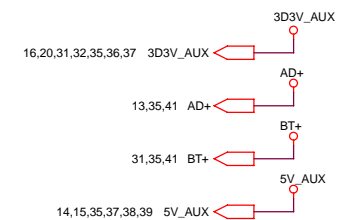
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
KEYBOARD/TOUCH PAD/Launch key			
Size	Document Number		Rev
A3	Leopard		-4
Date:	Monday, February 28, 2005		Sheet 32 of 41

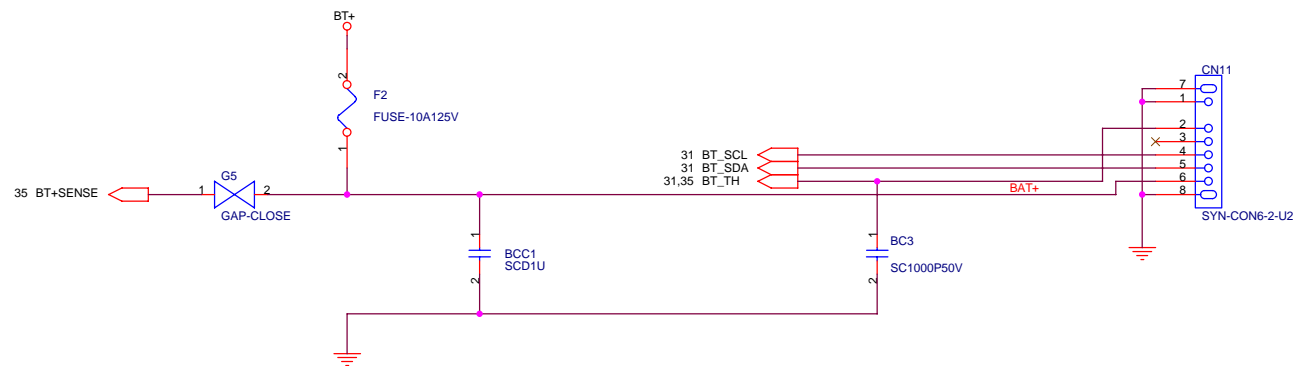


KBC_D[0..7] 31





BATTERY CONNECTOR

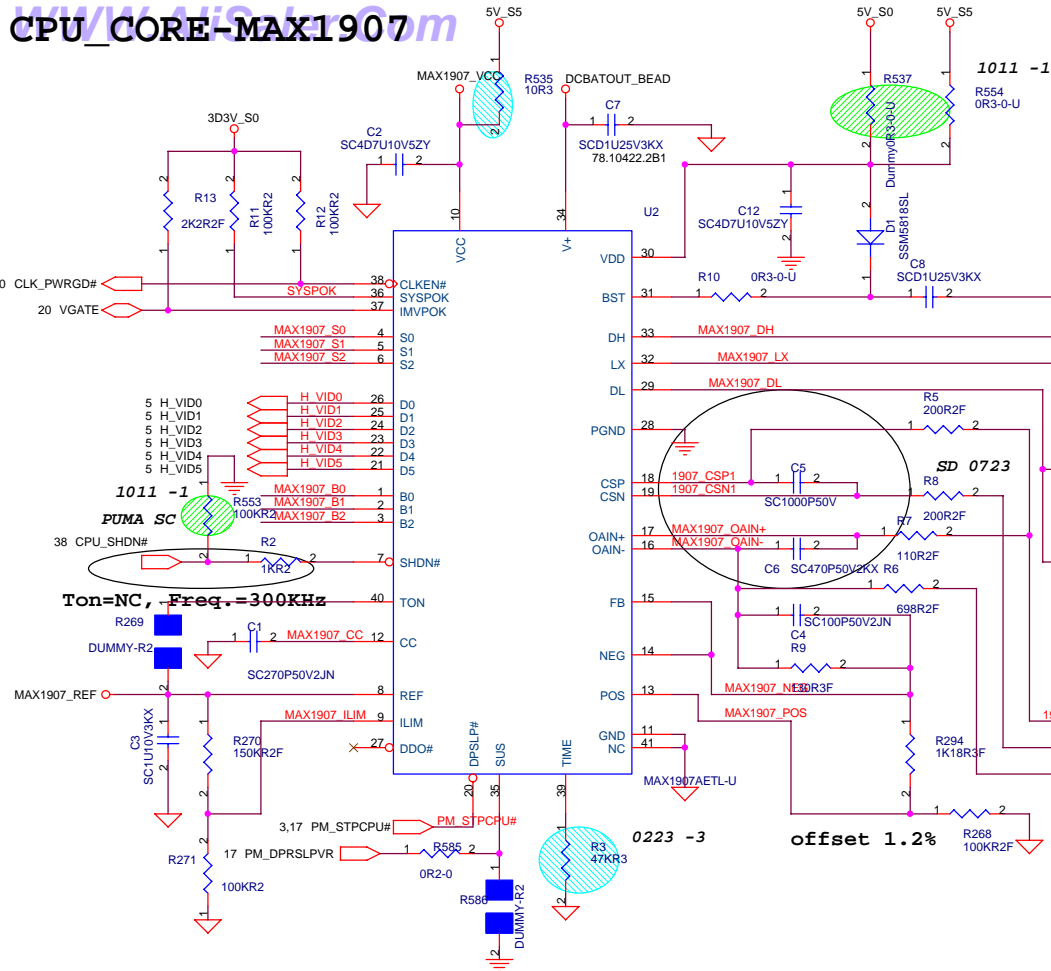




緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CHARGER MAX1999			
Size C	Document Number		Rev -4
		Leopard	
Date:	Monday, February 28, 2005	Sheet 35 of 41	

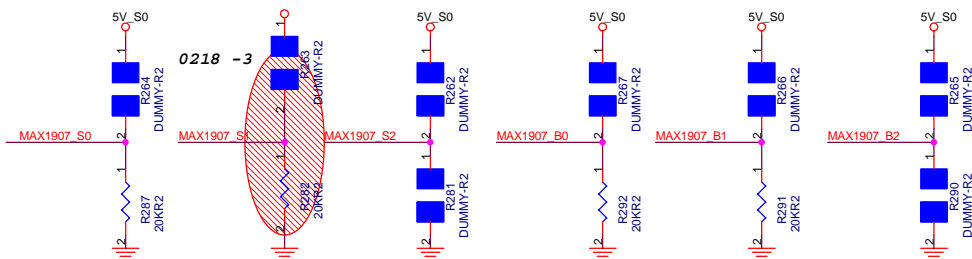
CPU_CORE-MAX1907



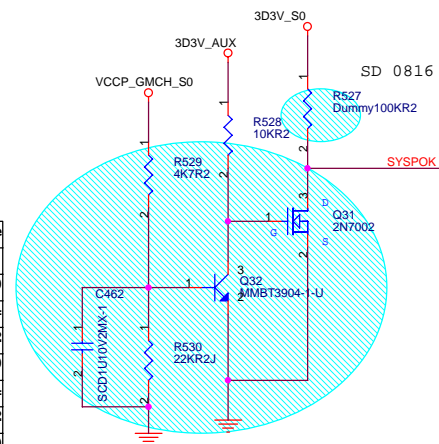
OCP=30A, Vally current = 27.5A,
Vilim=550mV(55mVp-p*10)

Deeper Sleep Voltage : 0.748V
, S0=L, S1=H, S2=Open,
5V_S0

Boot-up Voltage : 1.2V
, B0=L, B1=L, B2=Open



VID							Vcore
VID5	VID4	VID3	VID2	VID1	VID0	V	
0	1	0	1	1	1	1.340	
0	1	1	0	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	0	1	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	



SYSTEM DC/DC 3D3V_S5 / 5V_S5

3,5,7,9,11,13,14,16,17,18,19,20,21,22,23,24,25,27,29,30,31,32,36,38,40,41 3D3V_S0
17,18,19,21,25,29,31,35,39,40 3D3V_S5
16,20,31,32,34,35,36 3D3V_AUX
14,18,20,36,38 5V_S5
14,15,35,38,39 5V_AUX
14,35,38,39,40,41 DCBATOUT

3V = 4Arms,
OCP>6A

5V = 5Arms,
OCP>6.8A

These components should be
located near by MAX1977

These components should be
located near by MAX1977

ILIM5: $5V * 200K / (200K + 300K) = 2.0V$
 $200mV / 24 = 8.3A$
OCP point = $8.3A + 1/2Ripple$

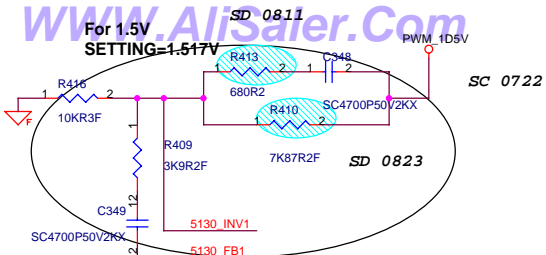
ILIM3: $5V * 200K / (200K + 300K) = 2.0V$
 $200mV / 24 = 8.3A$
OCP point = $8.3A + 1/2Ripple$
OCP point = $20A + 1/2Ripple$

ILIM*=Vcc 100mV
ILIM*=Vref 200mV
OCP= $0.1Vth/Rds(on) + 0.5Ripple$

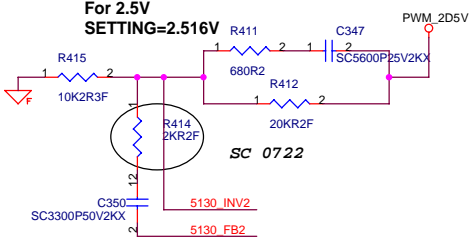
5V_S5 spec. = 10mA

SKIP# > 2.4V : PWM mode
SKIP# = GND(,0.8V) : SKIP MODE
SKIP# = REF (1.7V-2.3V)/Floating
Ultrasonic MODE(25KHz min)

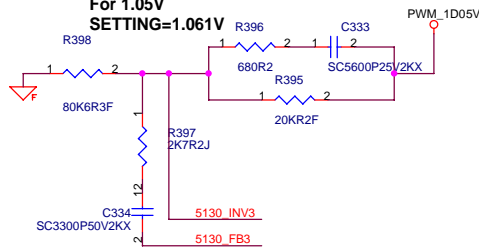
PM_SLP_S3# high = PWM
PM_SLP_S3# low = Ultrasonic



For 2.5V
SETTING=2.516V



For 1.05V
SETTING=1.061V



OCP 1.05V



OCP 2.5V



OCP 1D5V

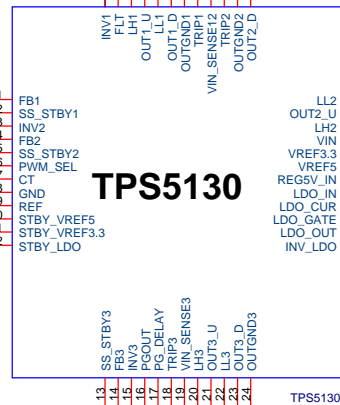


TI TPS5130 for 2.5V, 1.5V, 1.05V.

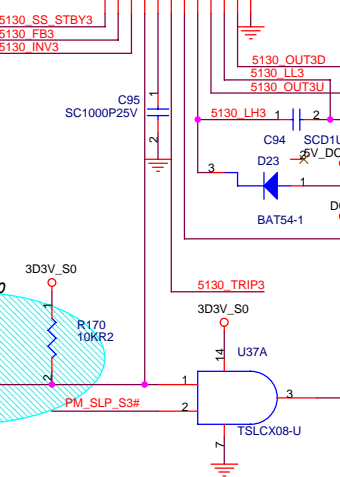
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

TPS5130

For 1.5V
SETTING=1.505V

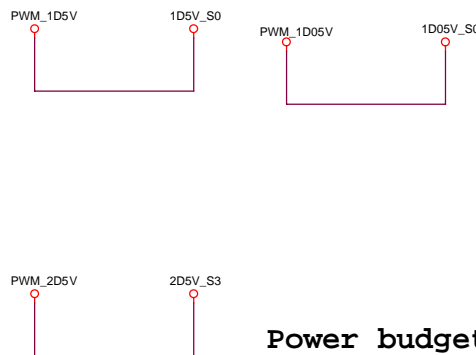
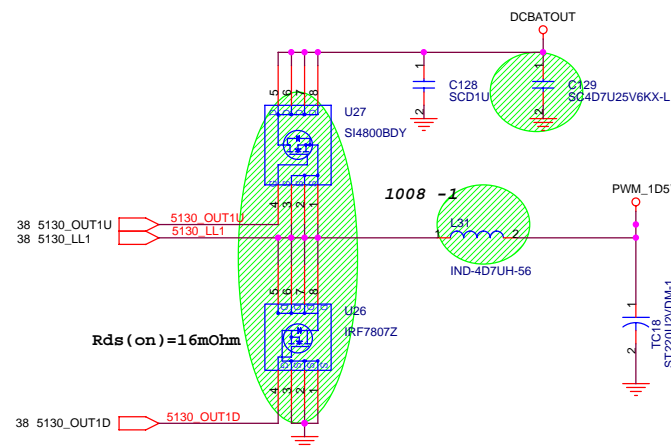


For 1.5V
SETTING=1.505V

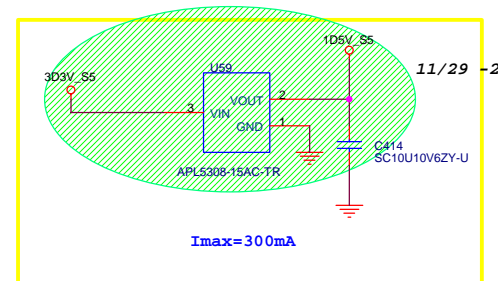


TI TPS5130 for 2.5V, 1.5V, 1.05V
(1D5V=>CH1 , 2D5V=>CH2 , 1D05V =>CH3)

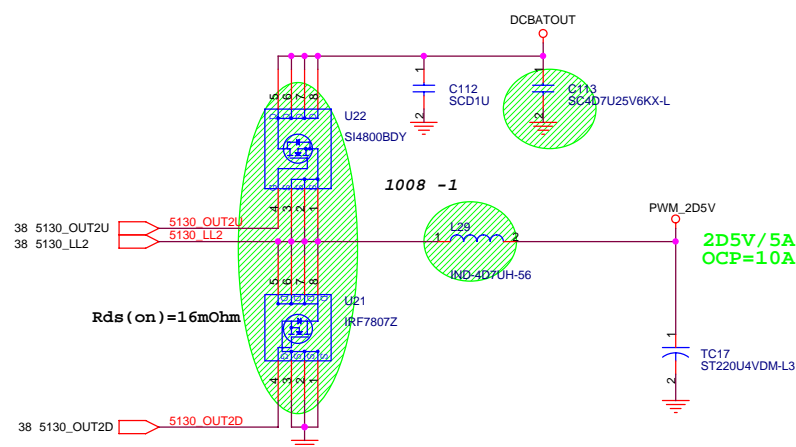
1D5V/5A
OCP=10A



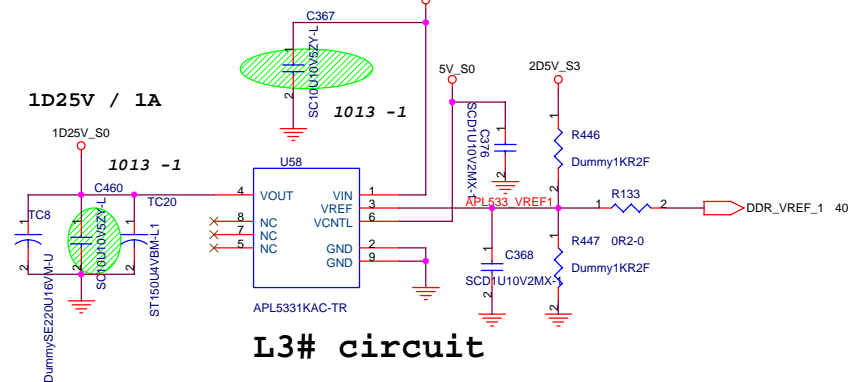
1.5V_S5 (For ICH6)



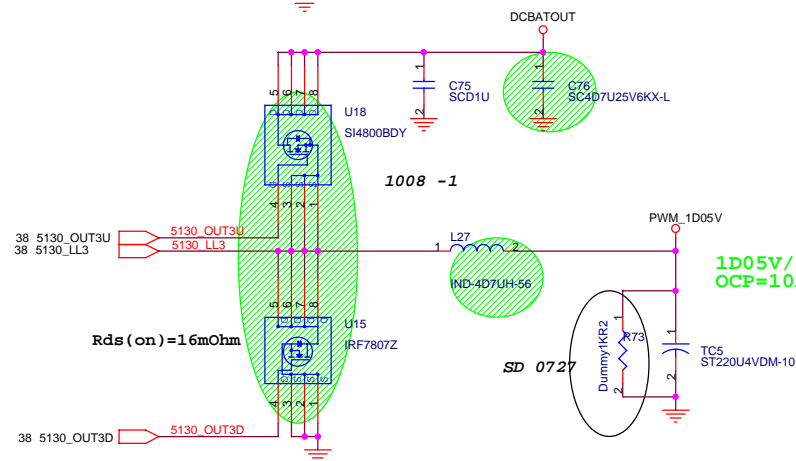
Power budget: 1.25V/2.2Apeak (For DDR1_VTT)



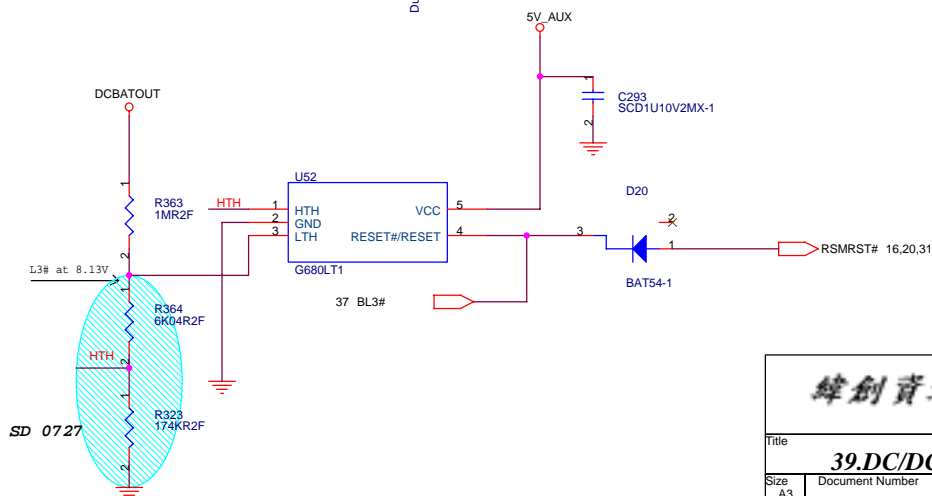
2D5V/5A
OCP=10A



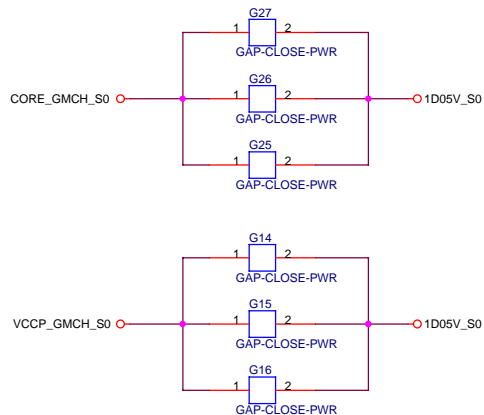
L3# circuit



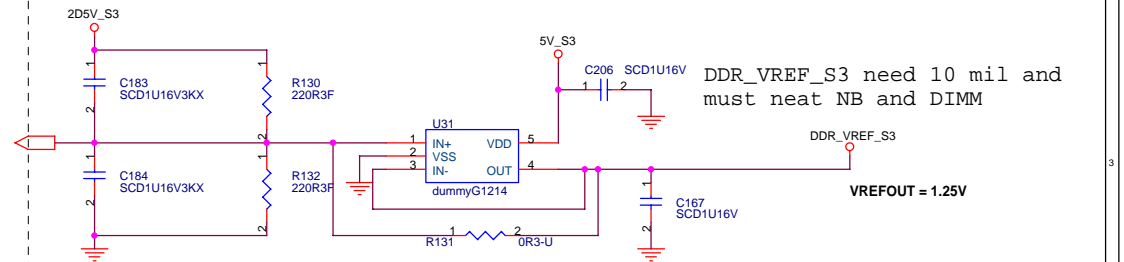
1D05V/5A
OCP=10A



FOR GMCH Power



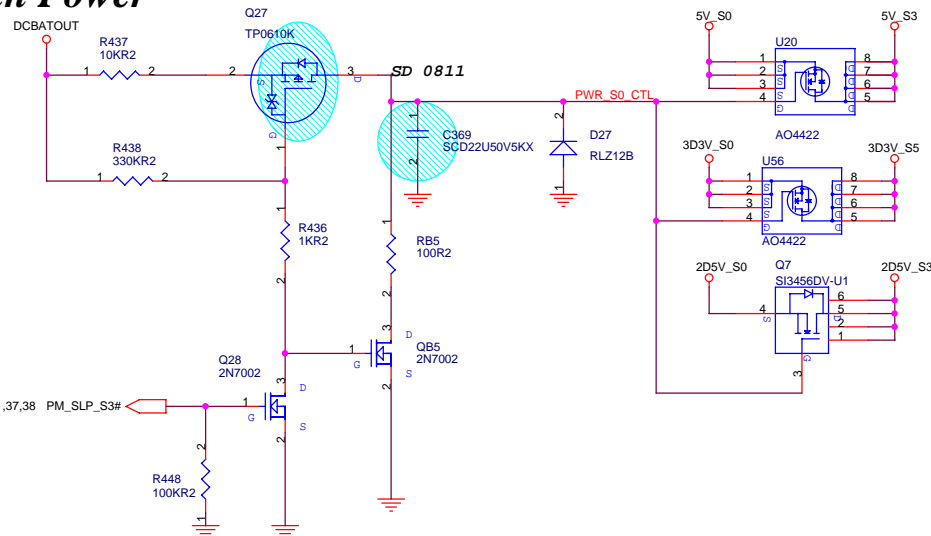
39 DDR_VREF_1



FOR DDR Power

Run Power

0223 -3



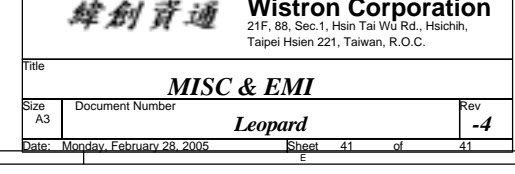
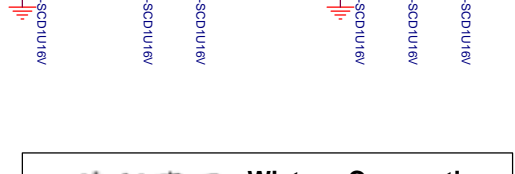
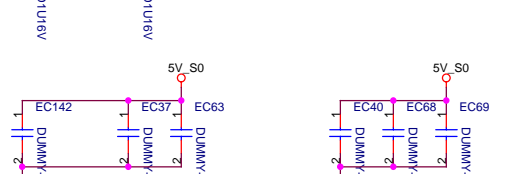
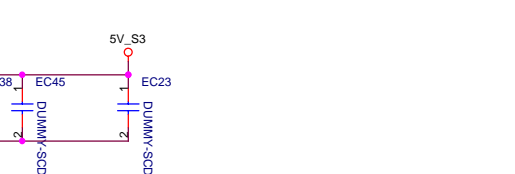
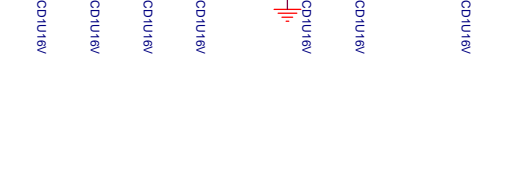
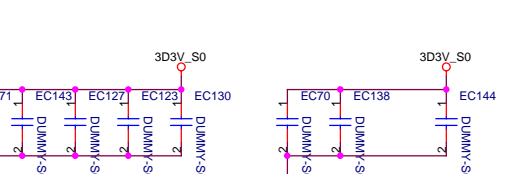
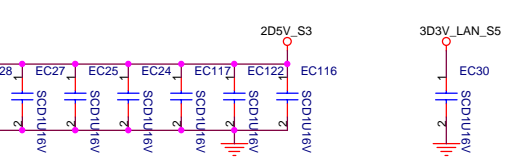
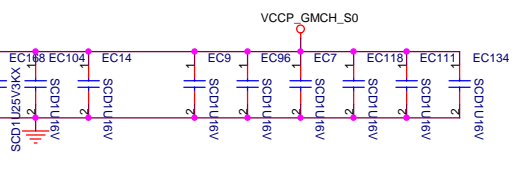
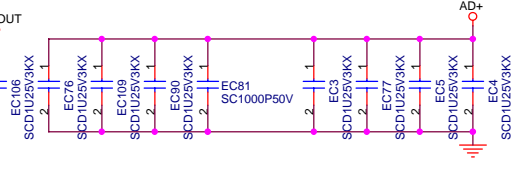
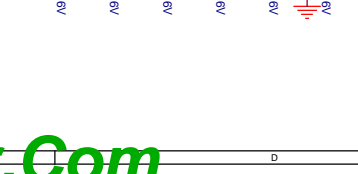
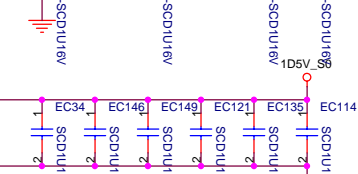
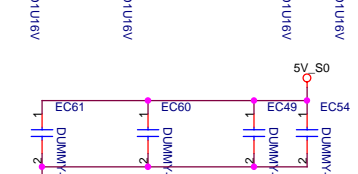
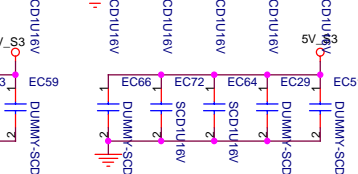
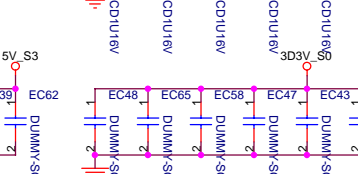
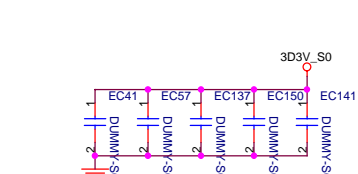
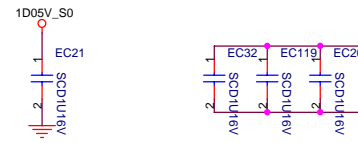
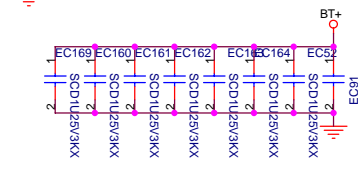
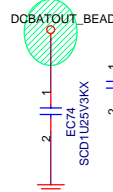
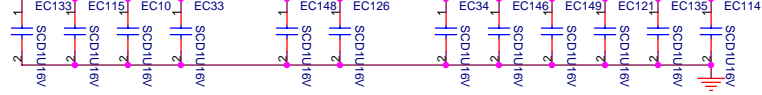
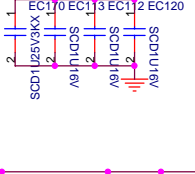
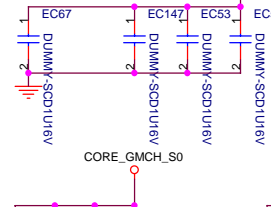
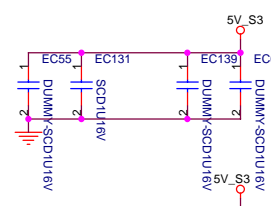
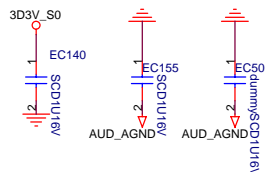
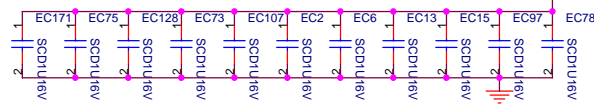
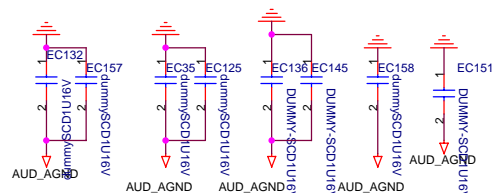
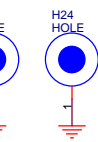
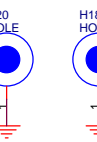
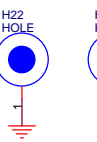
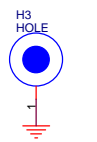
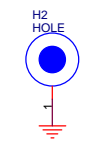
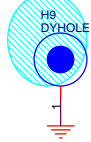
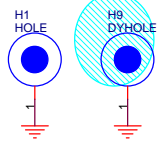
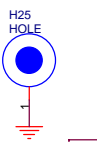
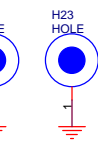
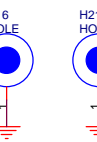
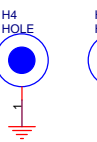
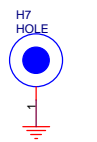
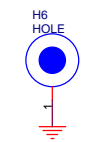
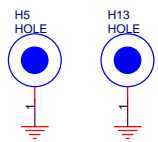
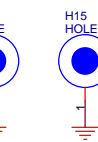
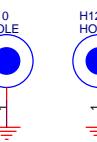
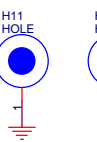
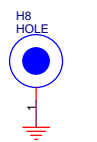
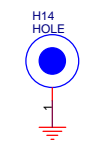
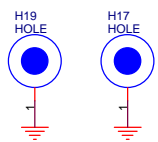
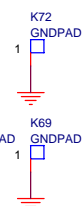
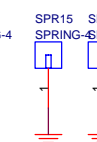
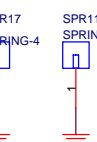
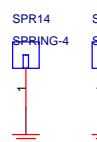
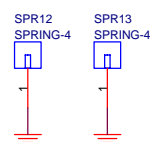
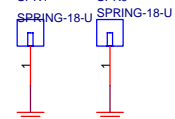
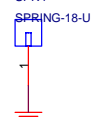
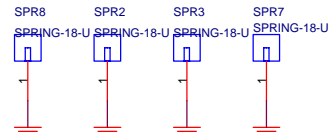
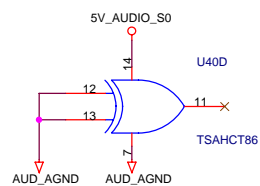
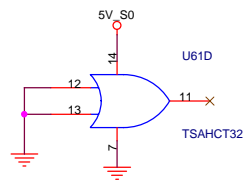
Suspend Power



緯創資通

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